Thermotest

Thermal test vehicle solutions by Nanotest

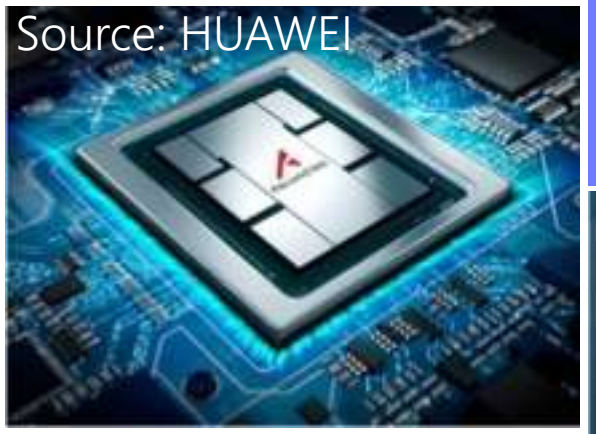
NANOTEST

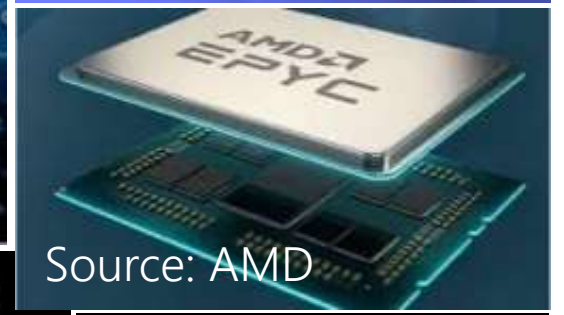
simply measured

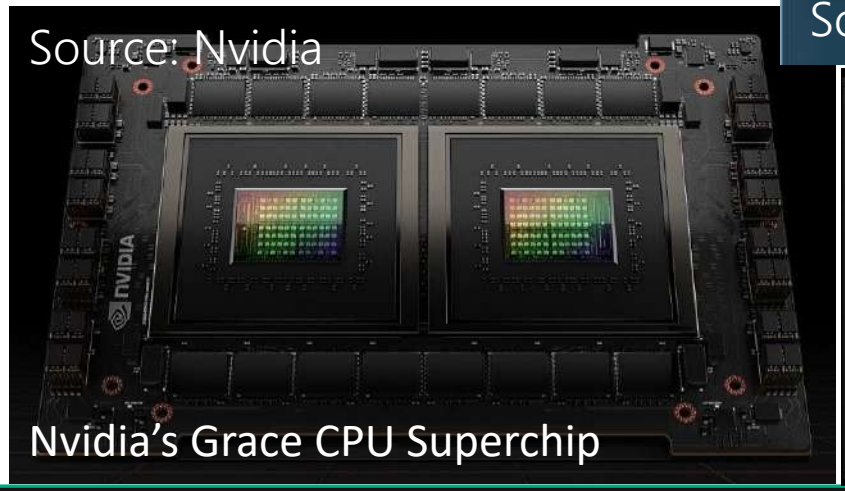
Motivation - what is thermal test vehicle

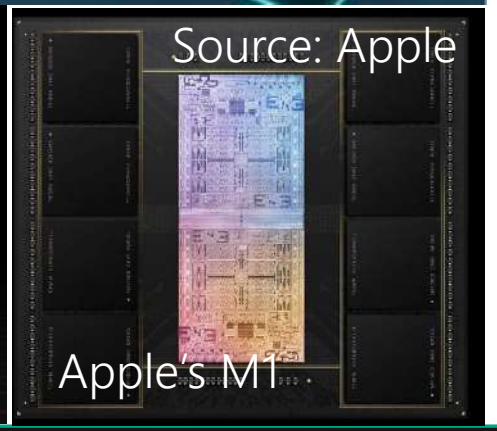
» **Thermal Test Vehicle (TTV)** is a Thermal Twin of a package (e.g., CPU, GPU or NPU) to investigate thermal characteristics of these packages

- Simulation of **hot spots and power density variation** and their impact on the package
- Investigation of **Thermal Interface Materials** (TIM1, TIM1.5 and TIM2) under real applications
- Development and investigation of **advance cooling solution** (Air cooling, liquid cooling, injection cooling etc.)
- **Reliability** investigation of packages
- Development and optimization of **assembly process**





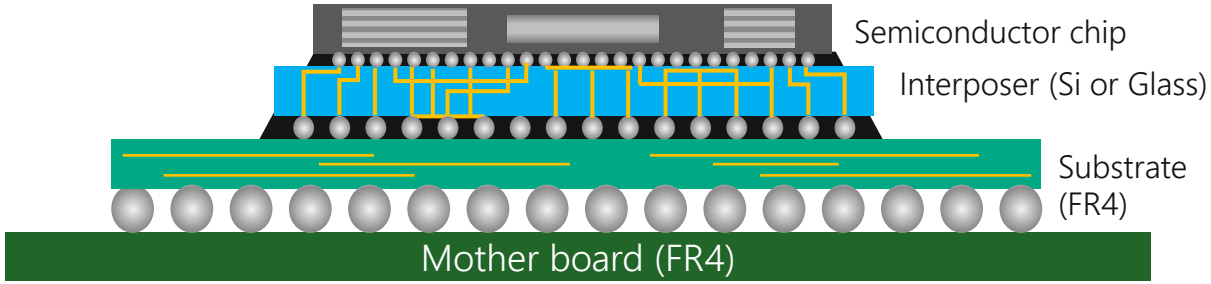




NANOTEST

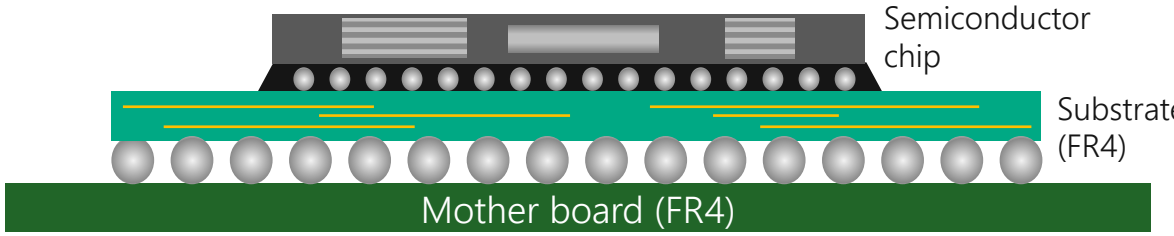
Package stack up

State of Art

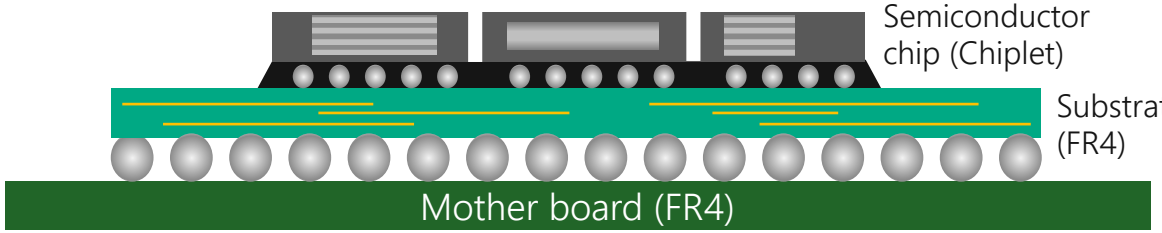


- **Using Si or glass Interposer :**
  - ++ Great CTE match between chip and interposer
  - ++ Low die warpage
  - - - Low signal density
  - - - High cost

Beyond State of Art



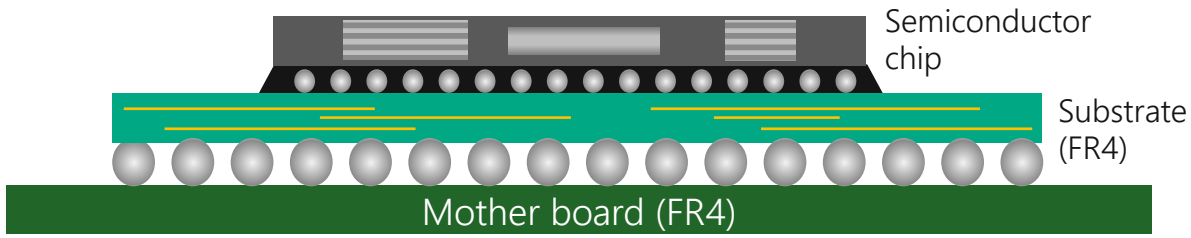
- **Using organic Interposer:**
  - - - CTE mismatch between chip and FR4 substrate
  - - - High die warpage → High stress on bumps
  - ++ High signal density
  - ++ Low cost

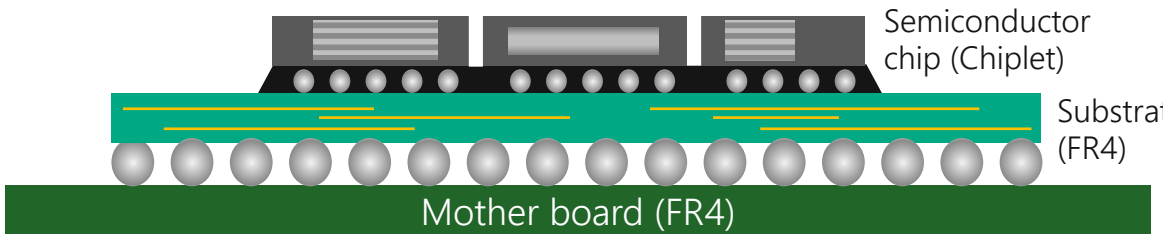


- **Using Chiplet:**
  - ++ Low warpage → low stress on bumps
  - ++ Large die possible
  - - - Challenging cooling

NANOTEST

What components are needed to build a TTV





1) Thermal test chip, which should have **temperature sensors** distributed across its surface and **heaters** allowing designing of hotspots and different heater zones
2) Substrates (Interposer and mother board)

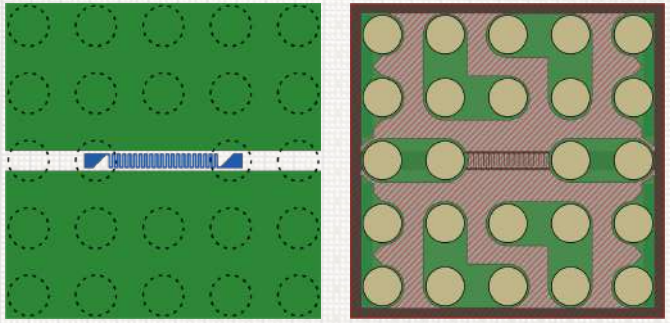
NANOTEST

Wafer

Thermal Test Chip Wafers by Nanotest

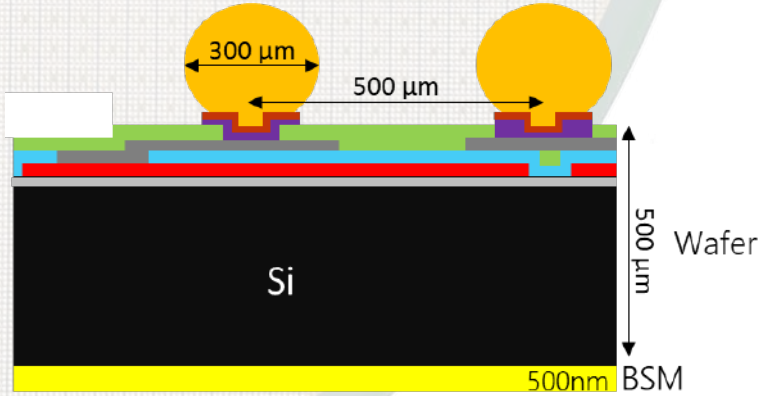
NANOTEST

Thermal Test Chip (TTC)



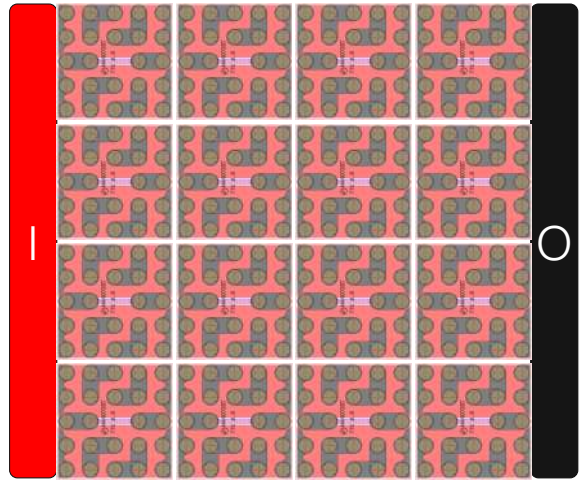
NT20-3k-FC

- Heater
- Sensor
- Solder Balls



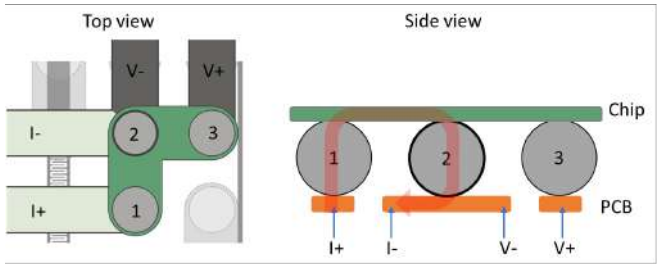
- 2.4 × 2.4 mm² unit cells
- 8" wafer / > 4000 cells
- 500 µm undoped silicon
- Flip-chip assembly
- 50 × 50 mm² max. die size*
- Backside metallized
  - Option 1: NiV 300 nm | Pt 100 nm | Au 200 nm
  - Option 2: Ti 100 nm | NiV 300 nm | Au 200 nm
  - Option 3: pure silicon
- Power density: up to 10 W/mm²
- RTD Sensitivity 10 Ω/K

grid connection



- **Example**
- 9.9 x 9.9mm² heating grid
- 7Ω resistance
- 10W/mm² => P=980W (11.8A/82.6V)
- Sensor location customizable

Resistive Bump Monitoring



*very risky and advanced technology

NANOTEST

Custom TTV Design and Manufacturing

Substrate, heat spreader, test board

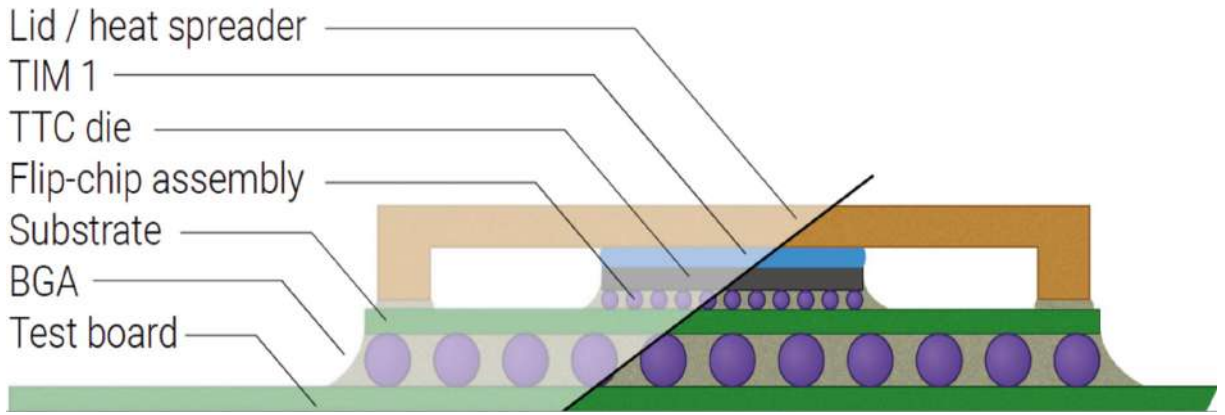
Thermal Test Vehicles (TTV)

Design the TTV you need. No Compromise

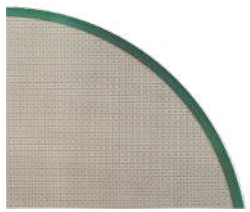
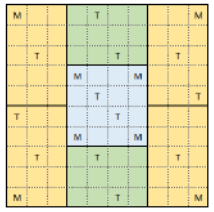
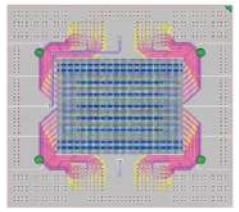
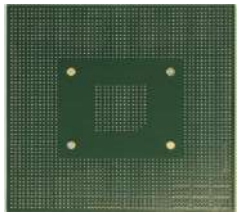
We support our customers to verify their prospective package, TIMs and cooling solutions by offering TTV solution

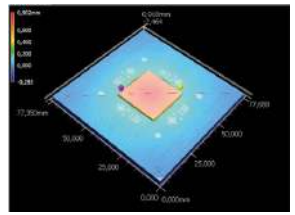
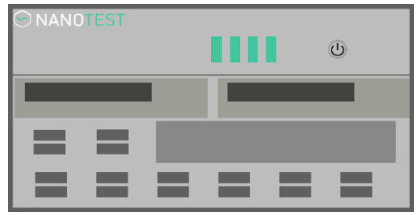
We offer:

- Thermal test chips wafer
- Concept and feasibility
- Interposer and test board
- Assembly and quality assessment
- Measurement hardware
- Measurement and control software
- Calibration and test



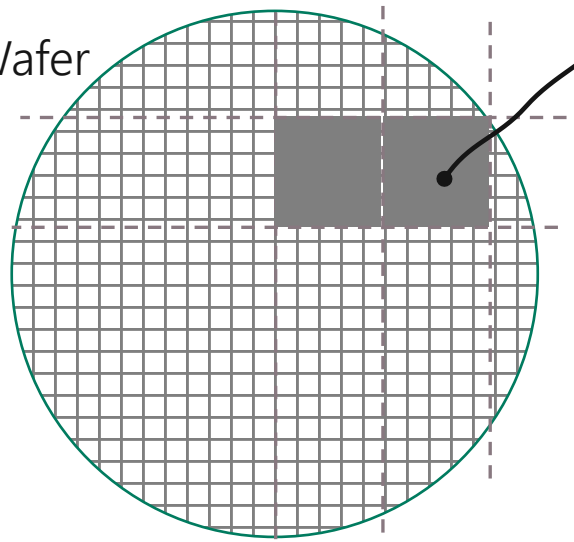
Thermal test chip wafer | Chip configuration | Substrate design | Substrate manufacturing | Chip and Board assembly | Quality control and test | Measurement hardware | Measurement Software

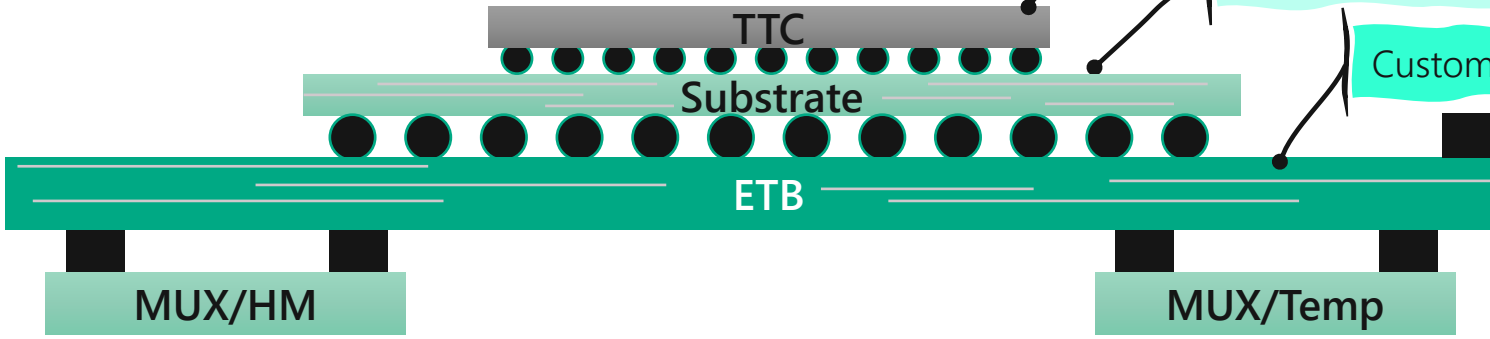




NANOTEST

We provide



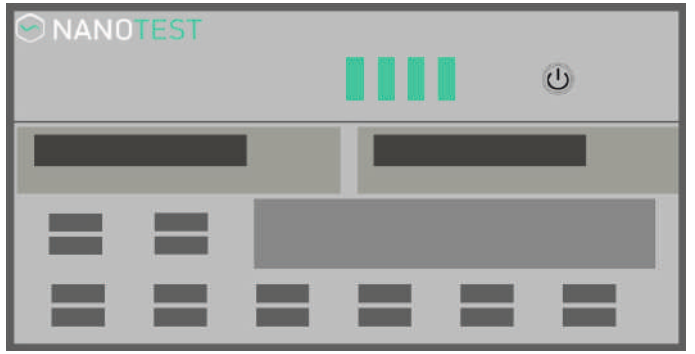
Customer specific die dimension



Customer specific die dimension

Customer specific substrate

Customer specific ETB



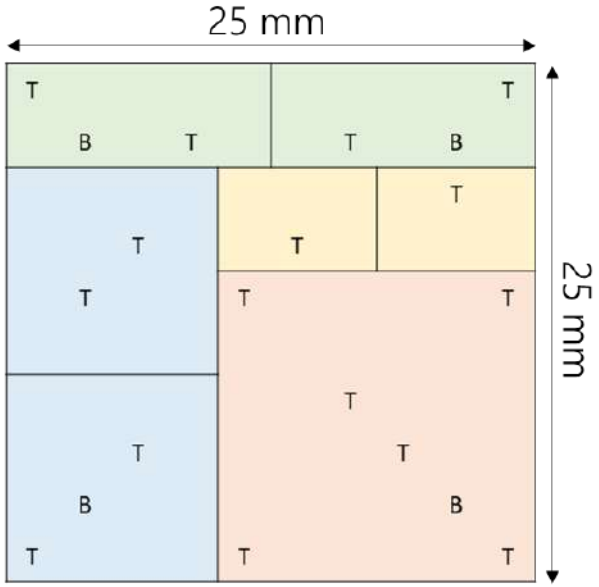
Measurement and control hardware

- Power supply
- Temperature measurement
- Monitoring bumps measurement
- Power control

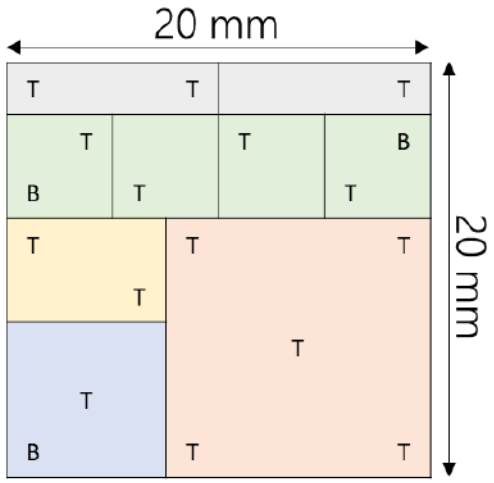
NANOTEST

Mapping Examples

Single Chip

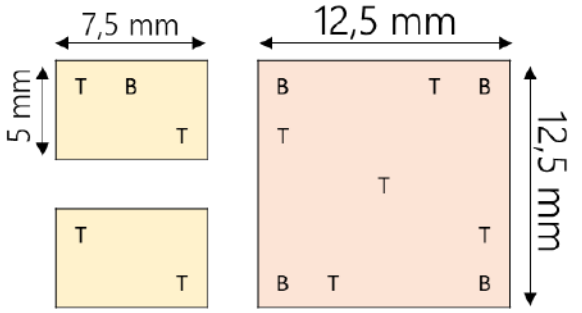


- 100 cells
- 625 mm²
- 7 power zones
- 16 RTD sensing
- 4 bump monitoring

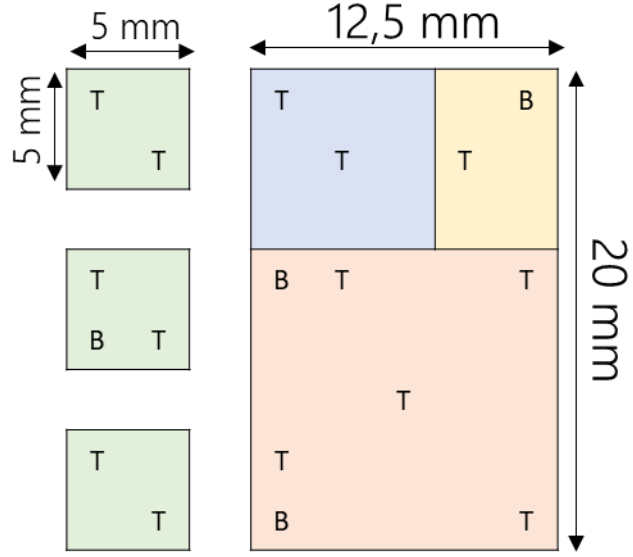


- 64 cells
- 400 mm²
- 9 power zones
- 15 RTD sensing
- 3 bump monitoring

Chiplet



- 37 cells
- 1x 156,25 mm²
- 2x 37,5 mm²
- 3 power zones
- 9 RTD sensing
- 5 bump monitoring



- 52 cells
- 1x 250 mm²
- 3x 25 mm²
- 6 power zones
- 14 RTD sensing
- 4 bump monitoring

NANOTEST

Interposer and substrate design

Customer specifications

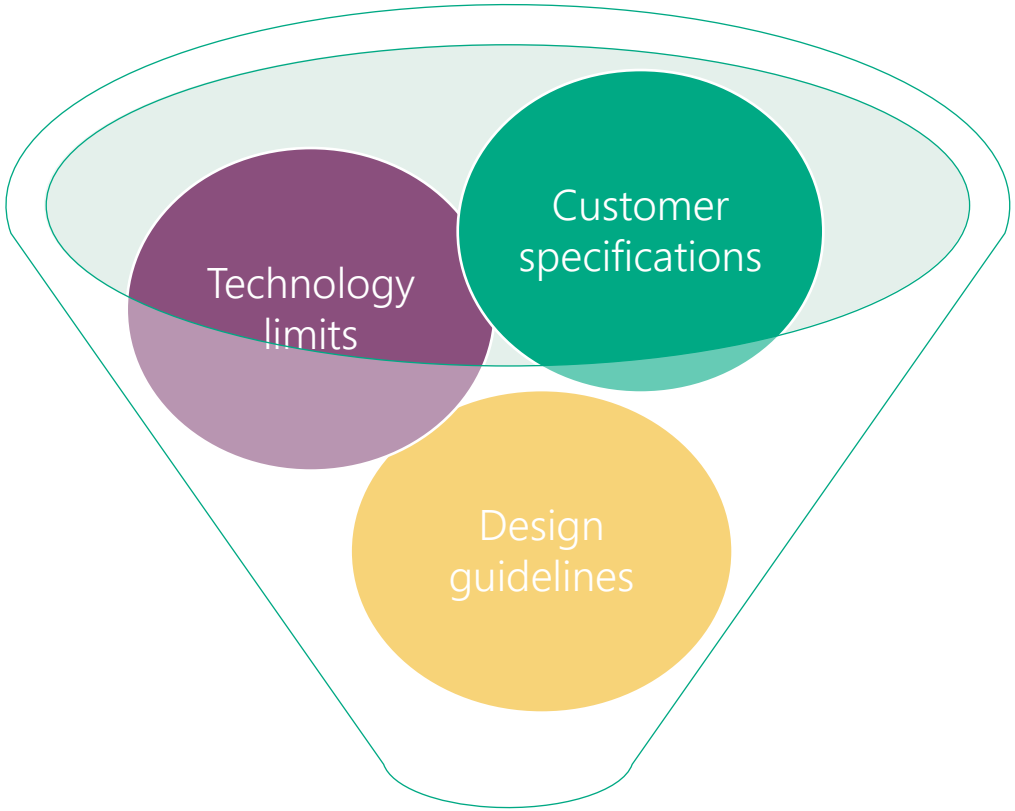
- Numbers of sensors and heater zone
- Substrate size
- Substrate thickness
- Number of layers and stack-up
- Interfaces

Technology limits

- Number of layers
- Vias technologies (through hole, blind vias, buried vias, micro vias)
- Line / space ratio
- Substrate material, copper thickness, substrate thickness

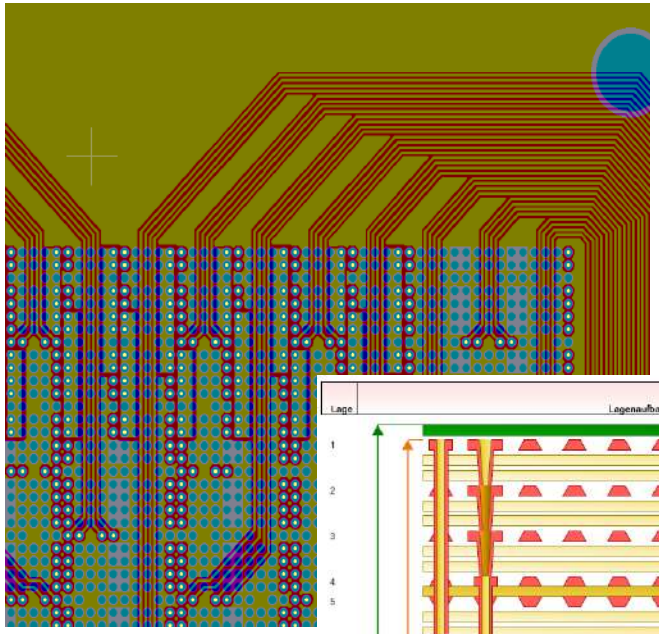
Design guidelines

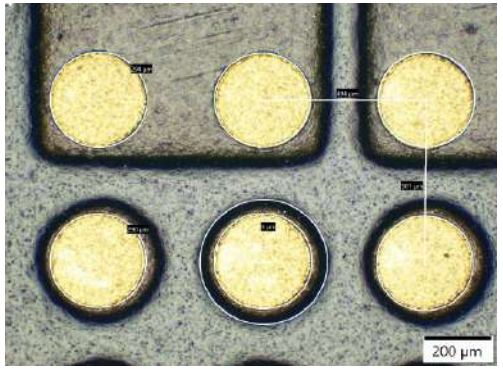
- Voltage, current limitation
- Routing density
- EMC
- Copper distribution
- Stack-up Symmetry

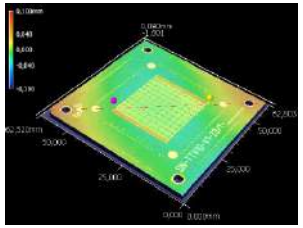


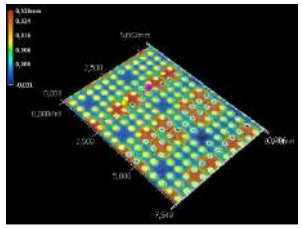
Optimized substrate

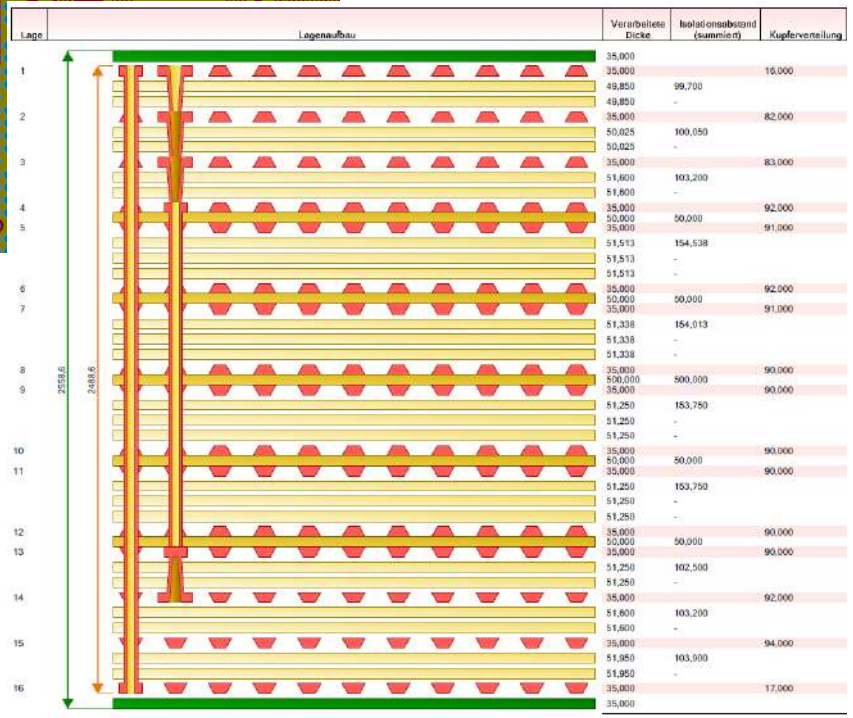
Substrate / Interposer









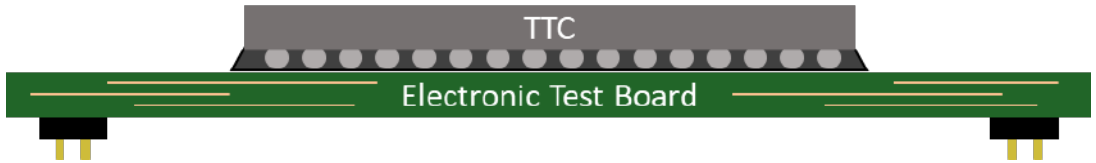


Requirements

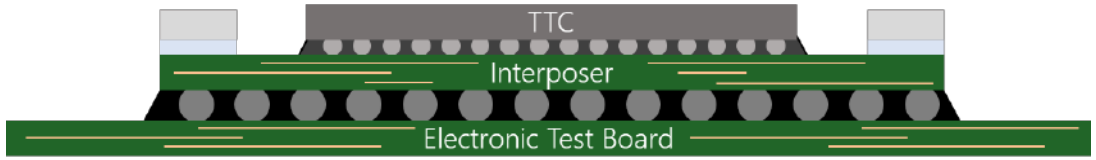
- Material (FR4, High TG, Low CTE)
- Dimensions (up to 100x100 mm²)
- Stack Up
  - Thickness (1.0 mm – 2.5 mm)
  - Number of layers (up to 16, 18, 20)
- Technology processes
  - Smallest structures (>100µm)
  - Copper thickness (18µm – 35µm)
  - Blind via, stacked via, buried via, via in pad
  - Filled and plugged (VII Filled and Capped-IPC 4761)
- Copper distribution

TTV System

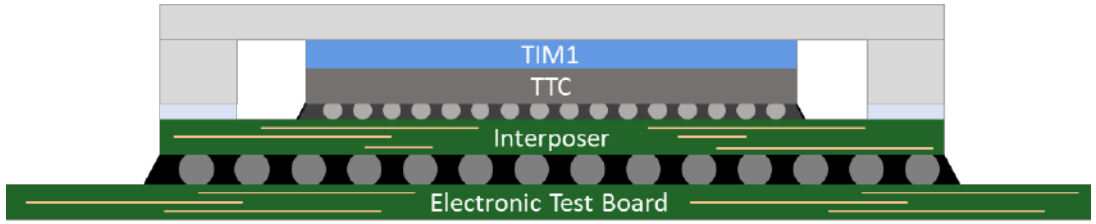
» Thermal Test Vehicle



TTV Package with connectors*

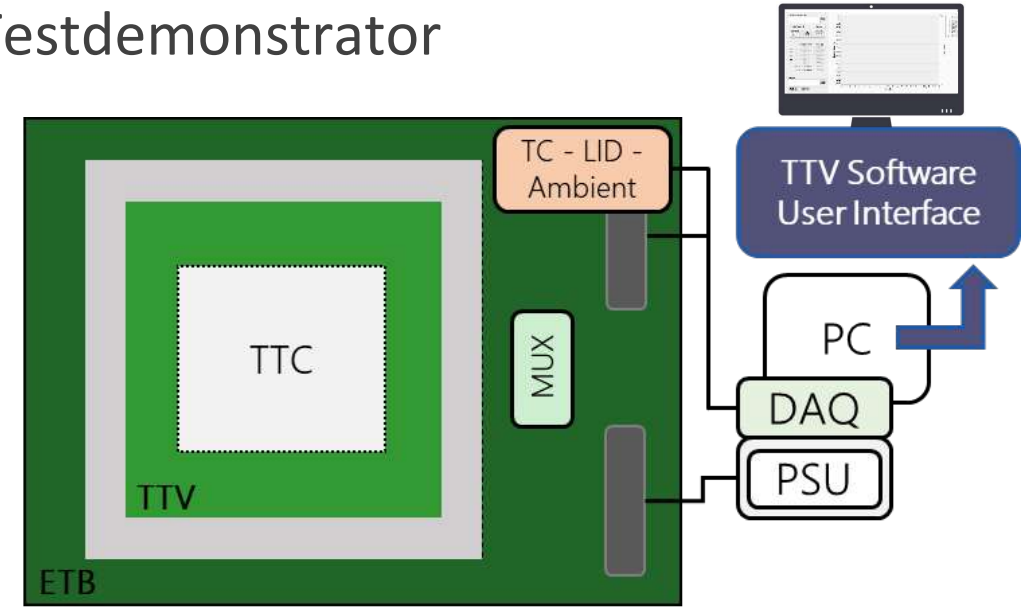


TTV Package with stiffener ring and BGA assembled on ETB*



TTV Package with LID + TIM material and BGA assembled on ETB*

» Testdemonstrator

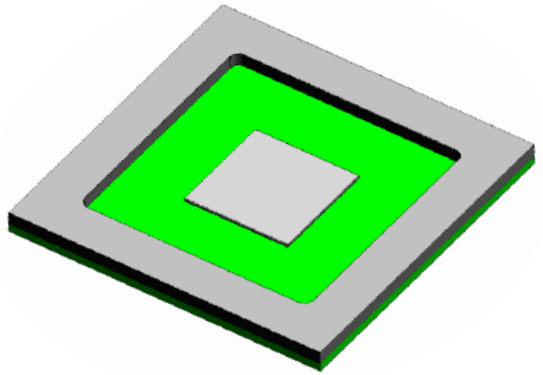


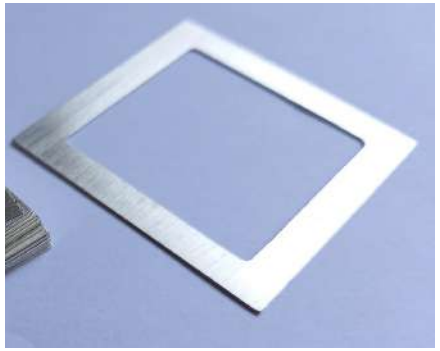
- » TTV Software for User Interface
  - › power dissipation control
  - › temperature visualization
- » Hardware Development/Implementation
  - › MUX for sensor multiplexing
  - › Power Supply
  - › DAQ system

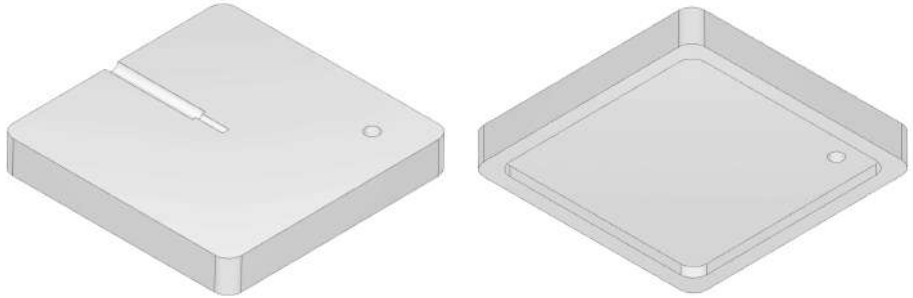
NANOTEST

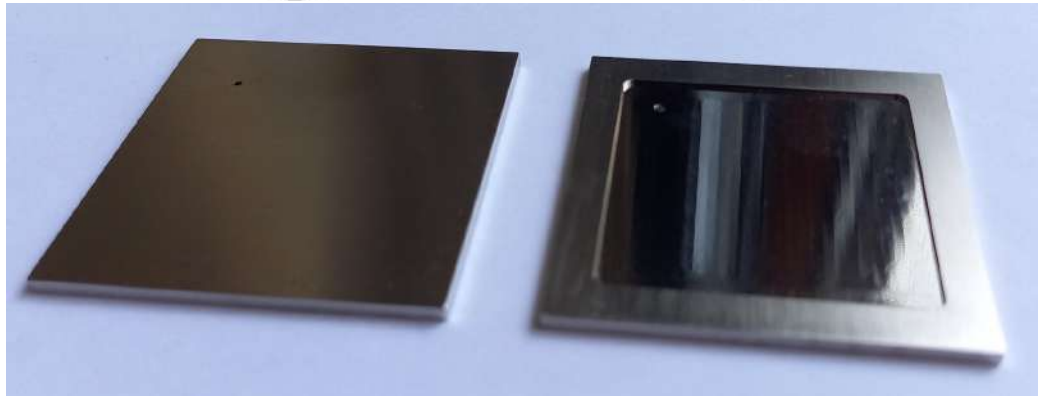
Heat spreader, Stiffener Ring and LID design

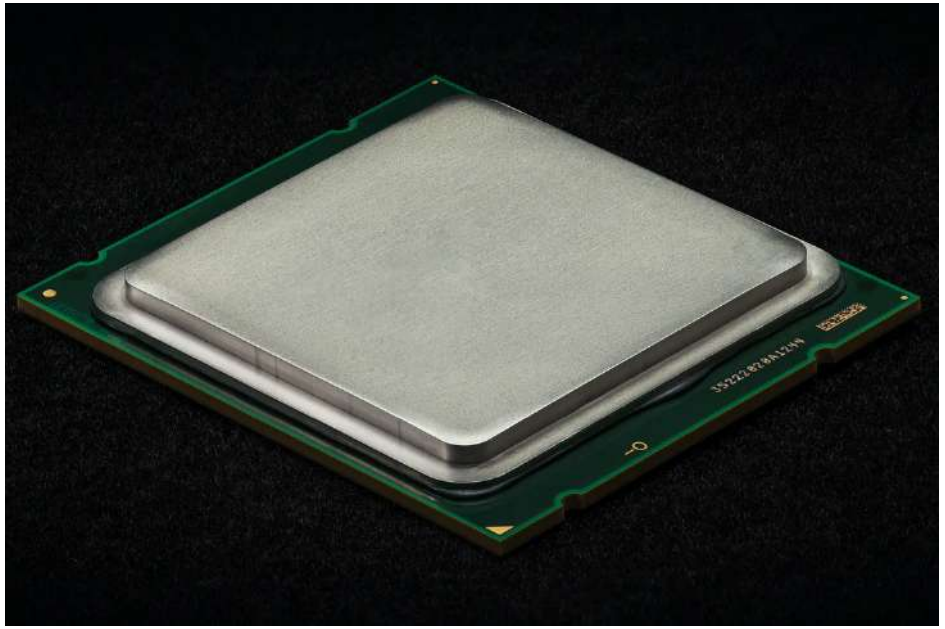
- Design according to customer specification
- Material: metal, alloy, coating, surface finish
- Geometry: size, TIM thickness
- Features: temperature sensors, cavities





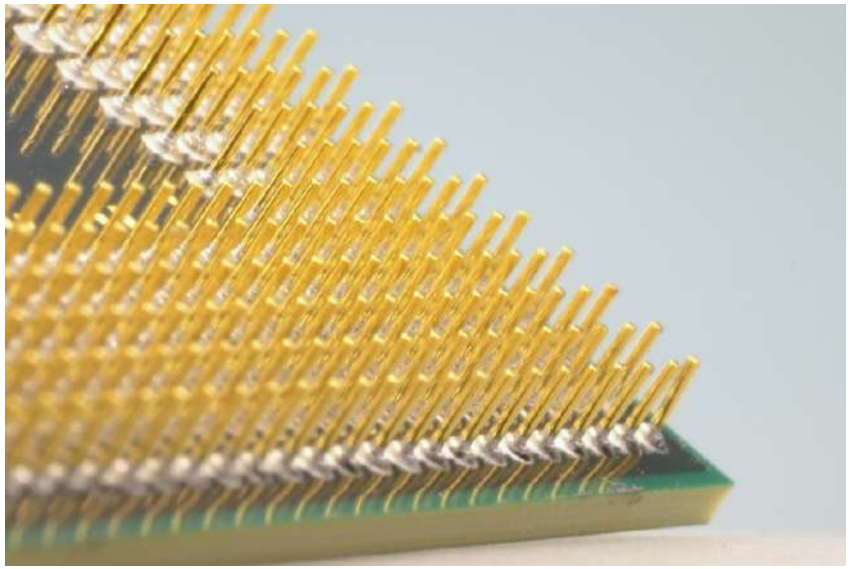


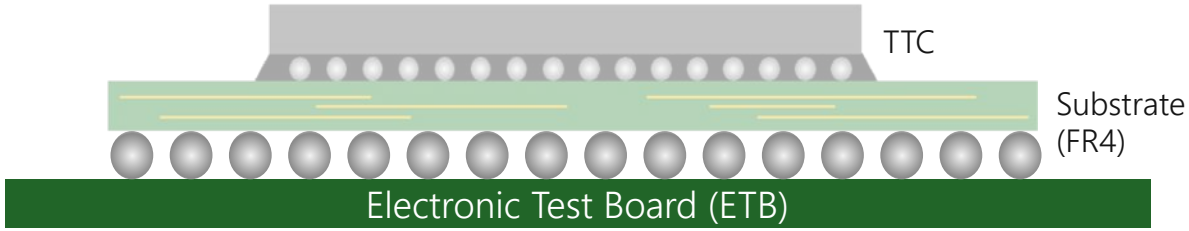




Electronic test board concept and design

- Electronic test board concept according to customer specification
  - TTV connection technology
    - BGA, LGA, PGA, SMT
  - Temperature measurement concept
    - I/O routing, probe current supply, MUX, interfaces
  - Heater supply routing
  - Mechanical design
    - Heat sink attachment, substrate fixation





NANOTEST

Assembly

TTV, heat spreader, test board

Process Flow I – Packaging and assembly capability

Wafer microscope
Olympus MX 63

Incoming inspection

Screen printer
DEK Galaxy

Solder application by stencil printing

Wafer microscope
Olympus MX 63

Optical inspection

Datacon 2200 evo advanced

Chip Assembling

GE nanome|x 180

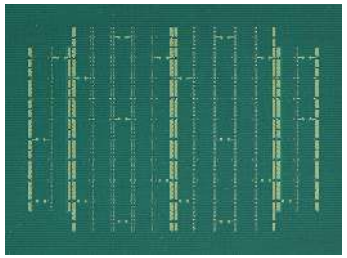
X-ray Inspection control of placement quality

Rehm Vision XS nitro 2100

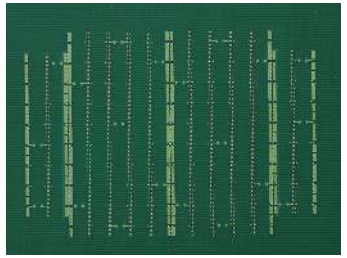
Reflow

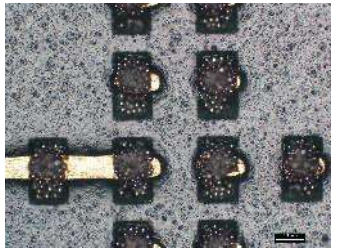
GE nanome|x 180

X-ray Inspection control of placement quality

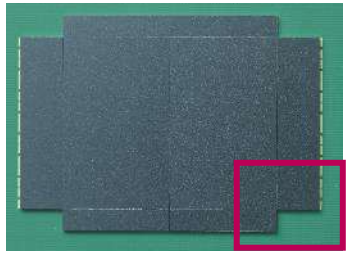


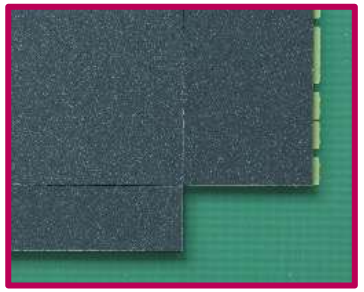
Initial state

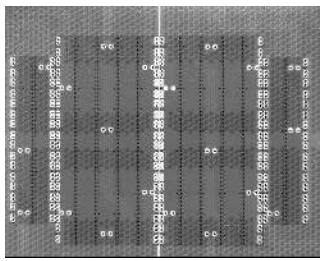


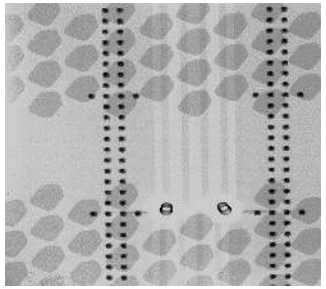


After printing application

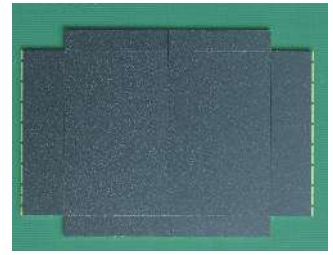


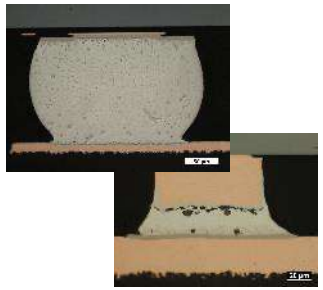


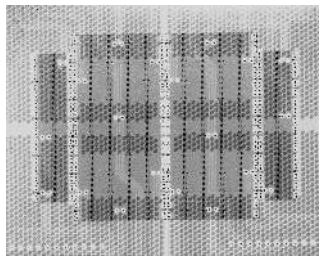


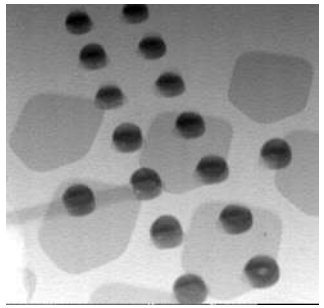


After chip placement







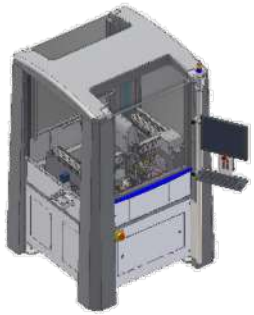


After soldering

In cooperation with

Fraunhofer IZM

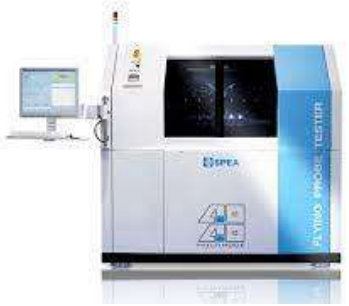
Process Flow II – Packaging and assembly capability



Infotech System FC1200

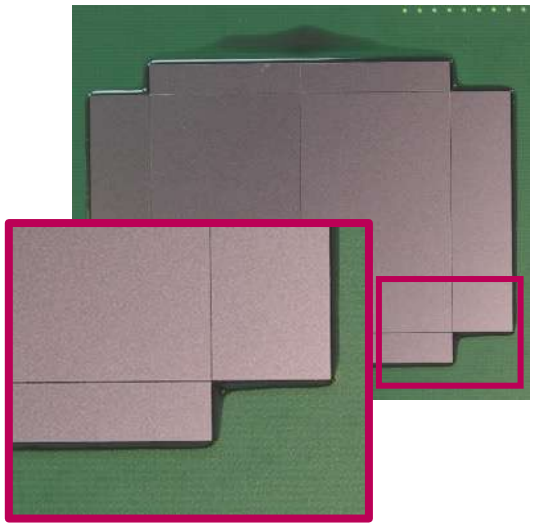
SONOSCAN GEN 6

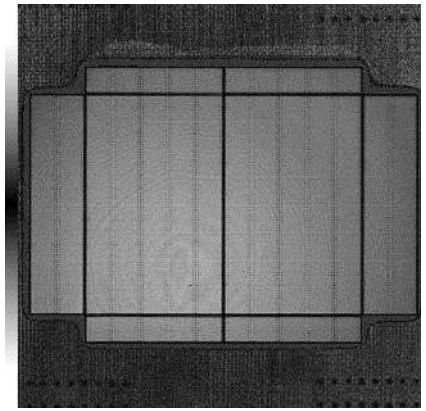
Wide Area 3D Measurement System VR 5200

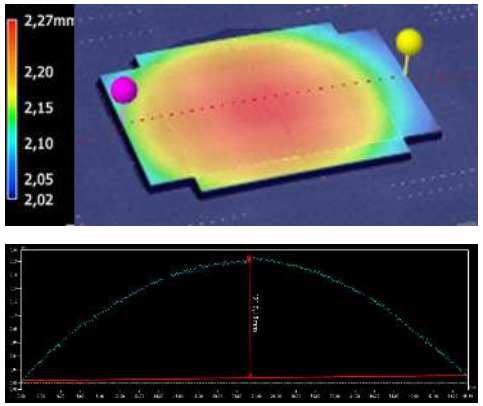


SPEA flying probe Tester 4040

Underfill	CSAM inspection	Optical inspection Warpage	Final electrical Test







After underfill

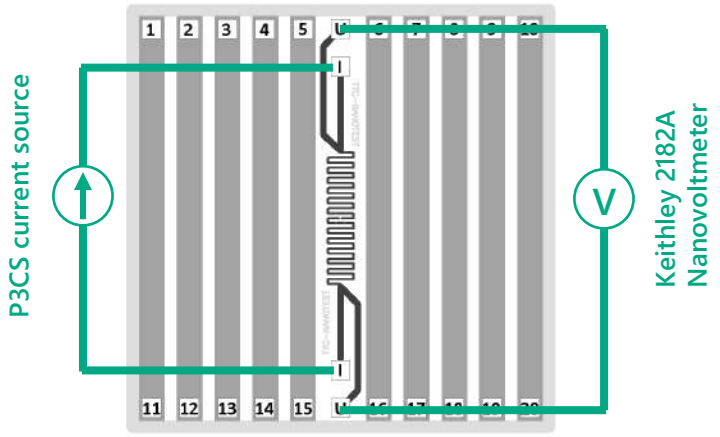
In cooperation with

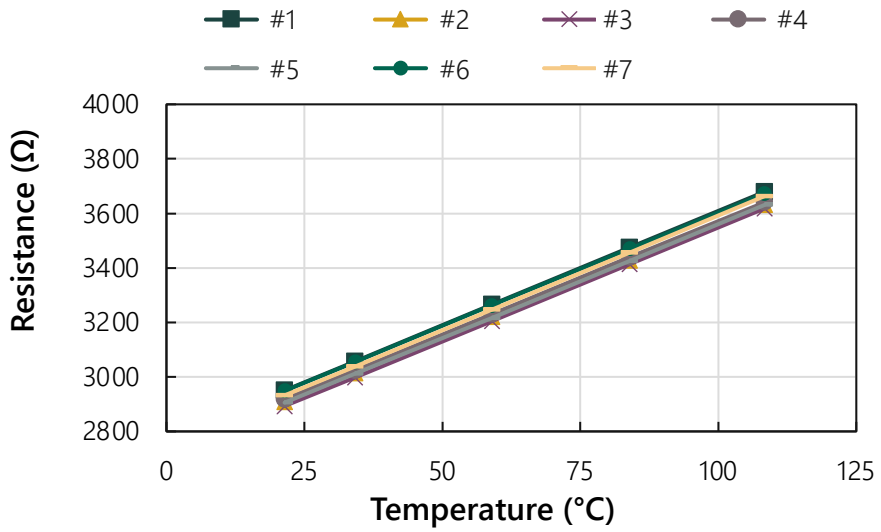
Fraunhofer IZM

Calibration and test

Temperature calibration

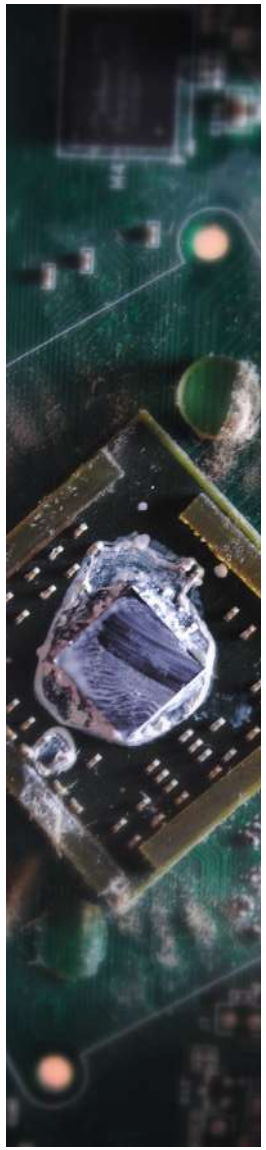
- Memmert universal oven UFE 500 (with forced air circulation)
- Resistance vs. temperature characteristics acquisition
  - 100 - 1000 µA probe current
  - 4-wire termination
  - I/V measurement for resistance determination
- Optional: TTV-specific multiplexers for process acceleration



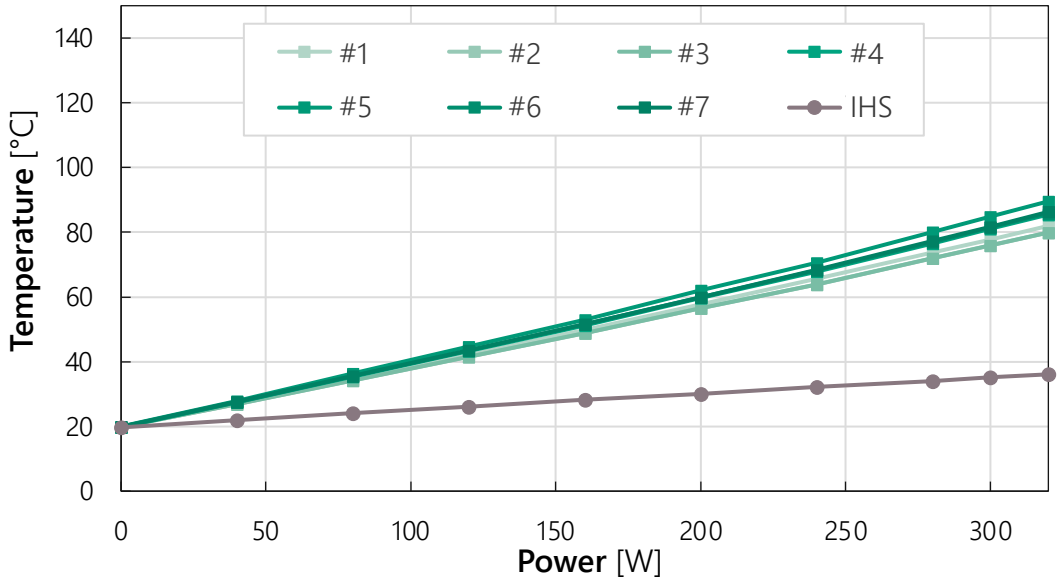


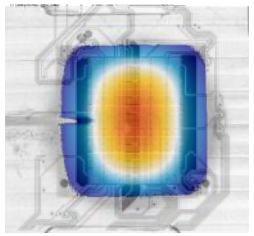
NANOTEST

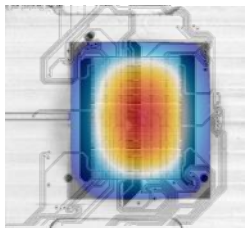
Testing

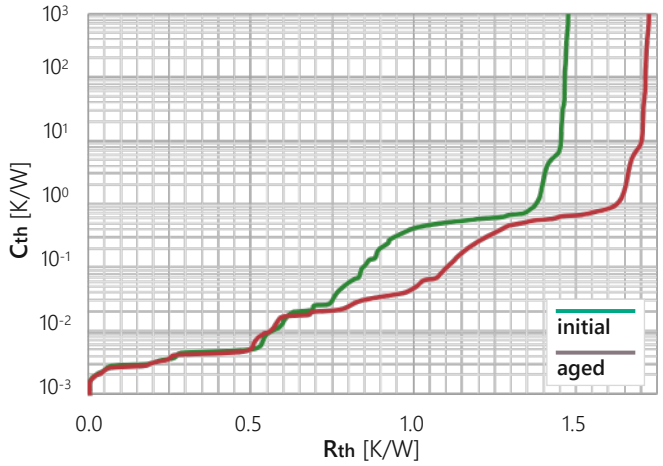


- Aging and stress tests
  - Temperature cycling
  - Thermal shocks
  - Power cycling
  - Climate chamber
- Measurement and analysis
  - On-chip temperature measurement
  - Thermographic hot spot detection
  - Thermal imaging-based failure analysis
  - Steady-state temperature profiling
  - Transient thermal analysis







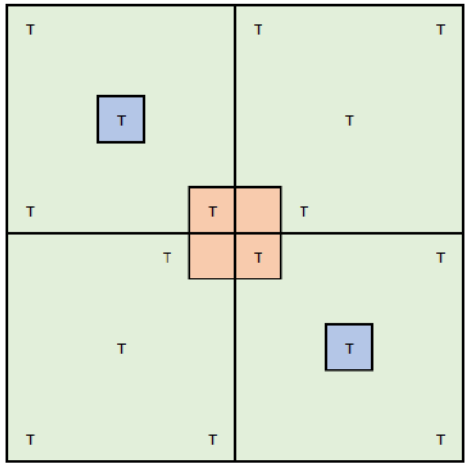


NANOTEST

Available TTVs and tools

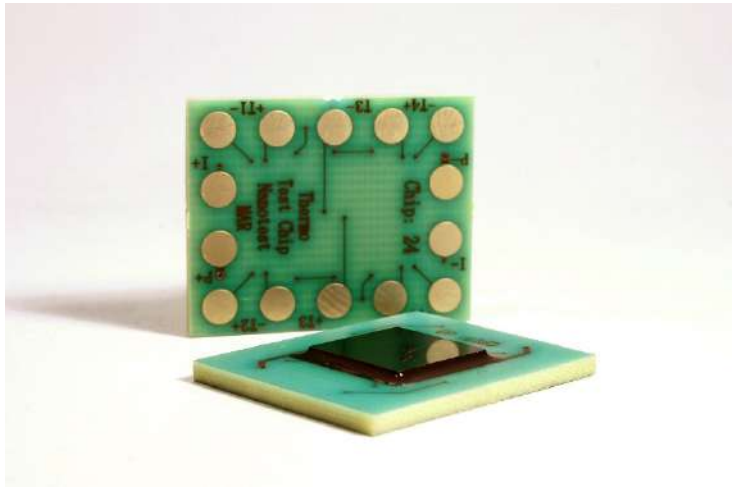
General purpose compact TTV

- Based on the NT20-3k-FC
- Chip dimension: 10 × 10 matrix | 24.9 × 24.9 × 0.5 mm^3
- Substrate dimension: 60 × 60 × 1.56 mm^3
- Package dimension: 60 × 60 × 2.24 mm^3
- Assembly technology: Flip chip and underfill
- Chip BSM: NiV 300 nm | Pt 100 nm | Au 100 nm
- 16 Temperature sensors (3.3 kΩ with 10.0 Ω/K sensitivity)
- 4 Independent heater zones (7 Ω each, 3.2 W/mm^2)
- Total package power: 2000 W



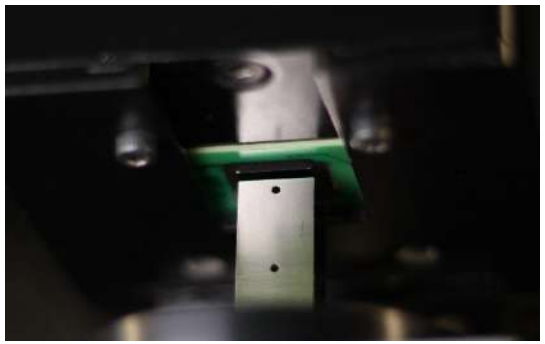
NT16-TTV5

» General purpose compact TTV

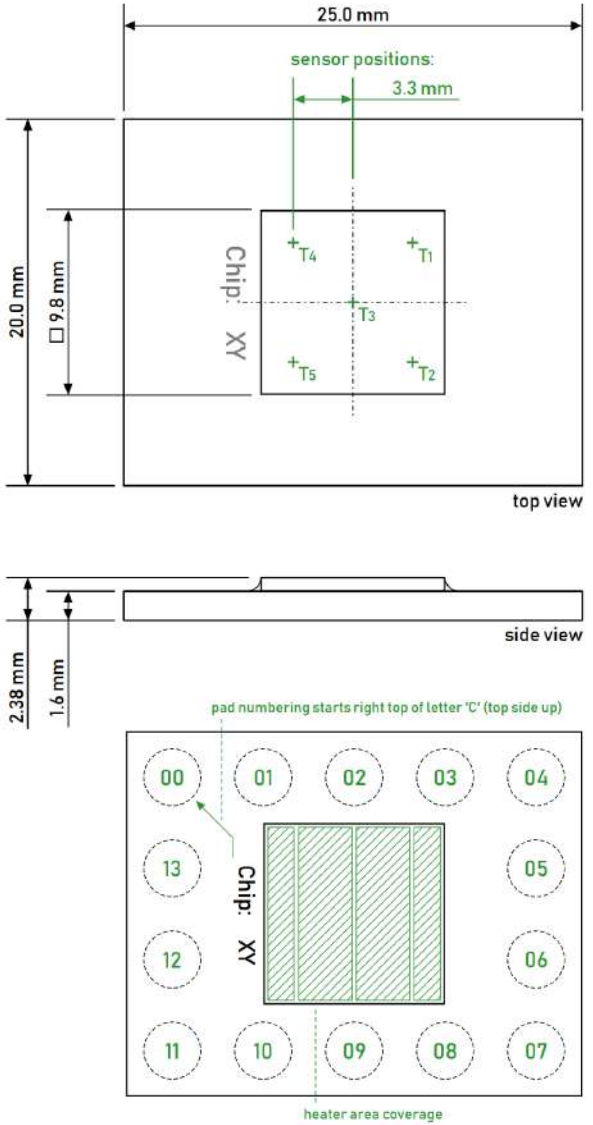


- **Based on the NT16-3k-FC**
- 3 × 3 matrix
- FR4 substrate, flip-chipped, underfilled
- Blank silicon surface
- 25 × 20 × 2.38 mm³ package
- Uniform resistor heater (15.5 Ω / 140 W max.)
- 5 RTDs (3.3 kΩ / 9 Ω/K)

Adhesive testing with TTV5

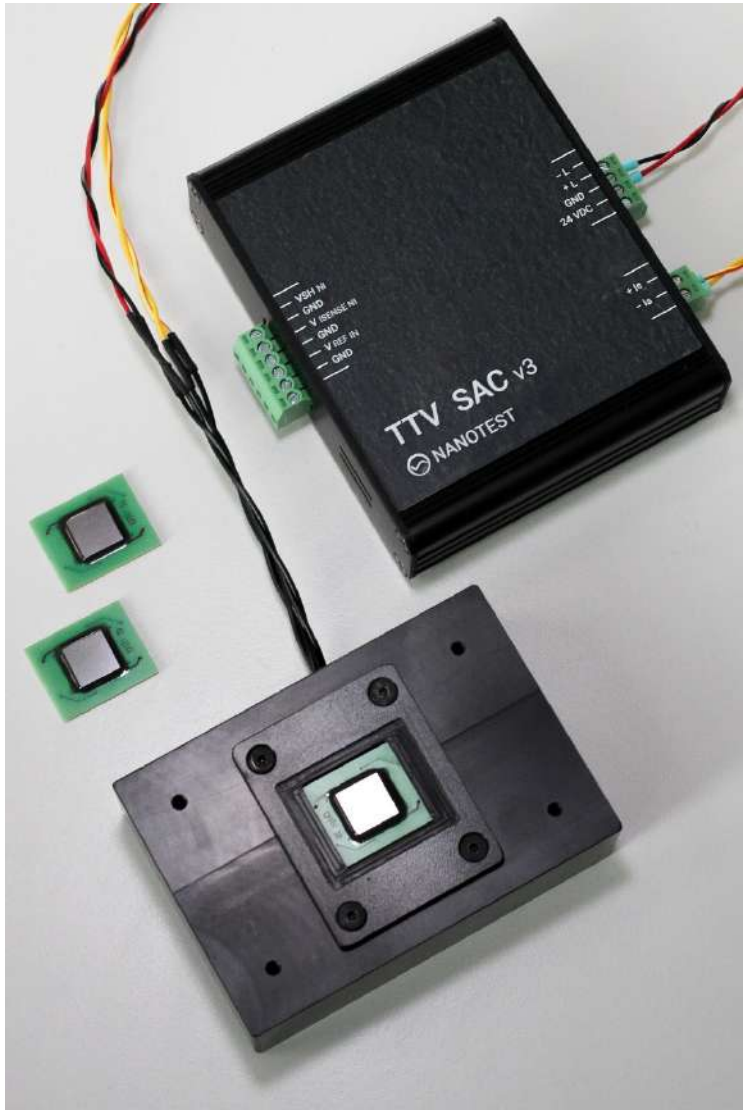


TIM1 characterization in TIMA® 5

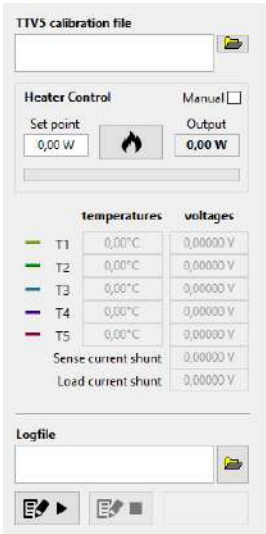


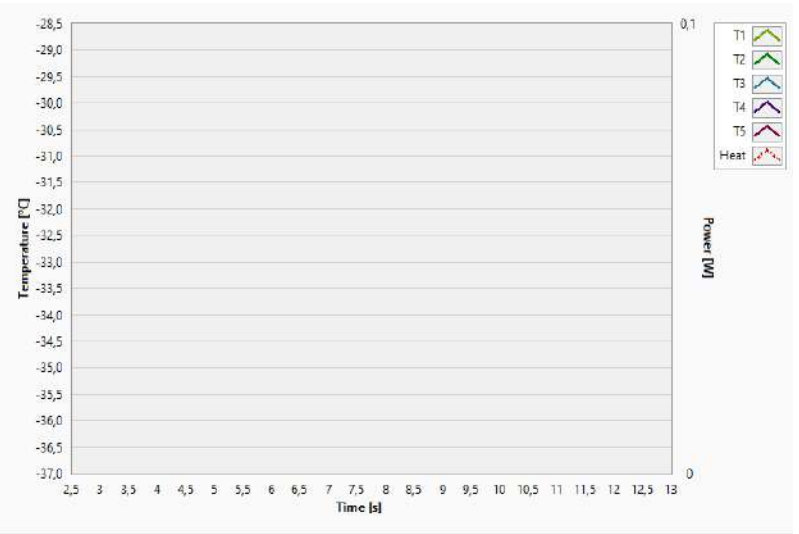
NANOTEST

Holder, electronics and Software for TTV5 (TTV5 SAC)



- **TTV Stand-Alone Controller v3**
- Hardware-software combination
- Designed for NT16-TTV5
- Features:
  - Heater control (automatic / manual)
  - Temperature monitoring
  - Logging
- Built for NT16-TTV5
  - Foundation for customization
  - Adaptable to any small-scale TTV





NANOTEST

NANOTEST

simply measured

Thank you

nanotest.eu

Berliner Nanotest und Design GmbH
Volmerstr. 9 B, 12489 Berlin, Germany
info@nanotest.eu +49 30 6392 3880