

Thermal Test Chips & Thermal Test Vehicles

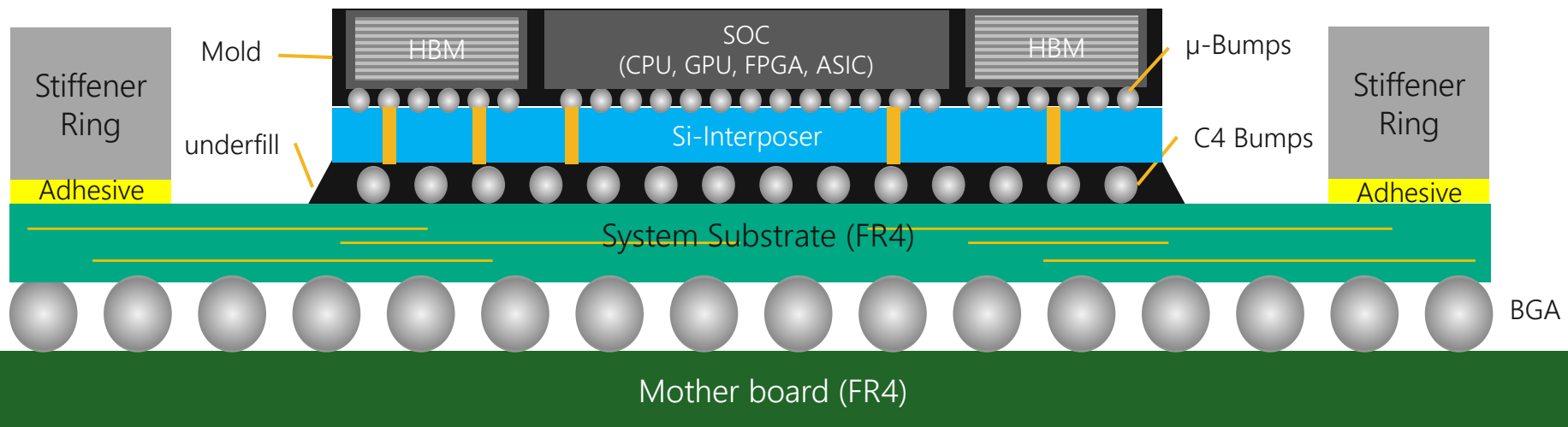
A NANOTEST SOLUTION



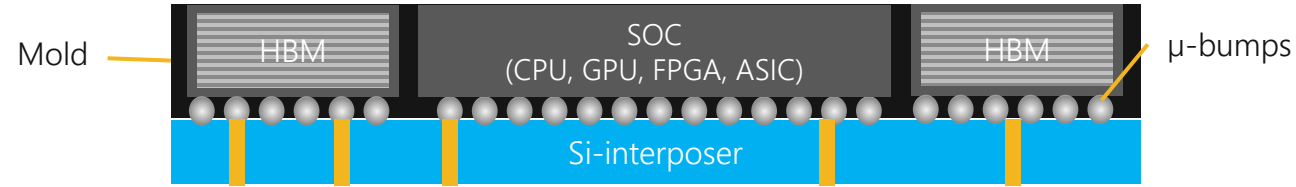
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TTV | Thermal Test Vehicle

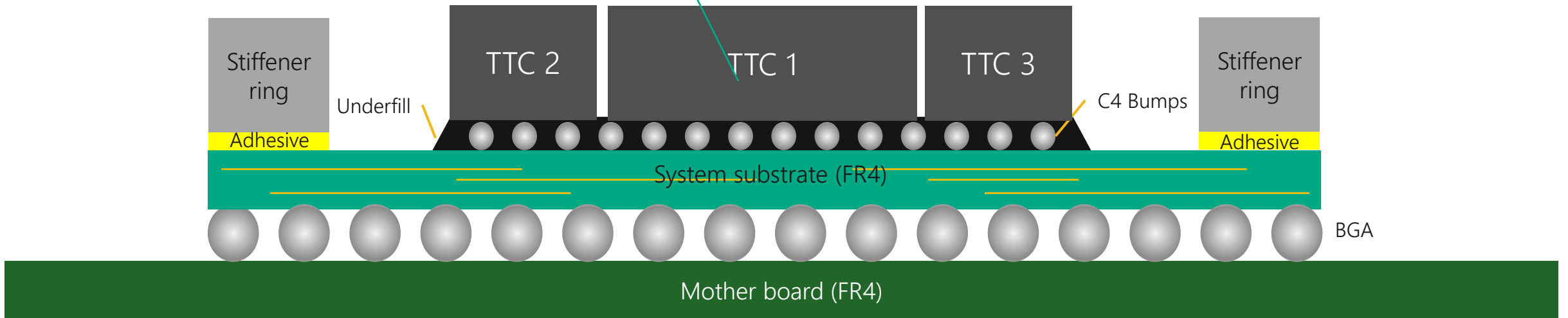
- » **Thermal Test Vehicle (TTV)** is a thermal twin of a package (e.g., CPU, GPU or NPU) to investigate thermal characteristics of these packages
- » Simulation of **hot spots and power density variation** and their impact on the package
- » Investigation of **Thermal Interface Materials** (TIM1, TIM1.5 and TIM2) under real applications
- » Development and investigation of **advanced cooling solutions** (air cooling, liquid cooling, injection cooling etc.)
- » **Reliability** investigation of packages
- » Development and optimization of **assembly process**



- TTCs: adjustable size, controllable heat loss in defined heating zones and localised temperature measurement
- Real die does not have these features



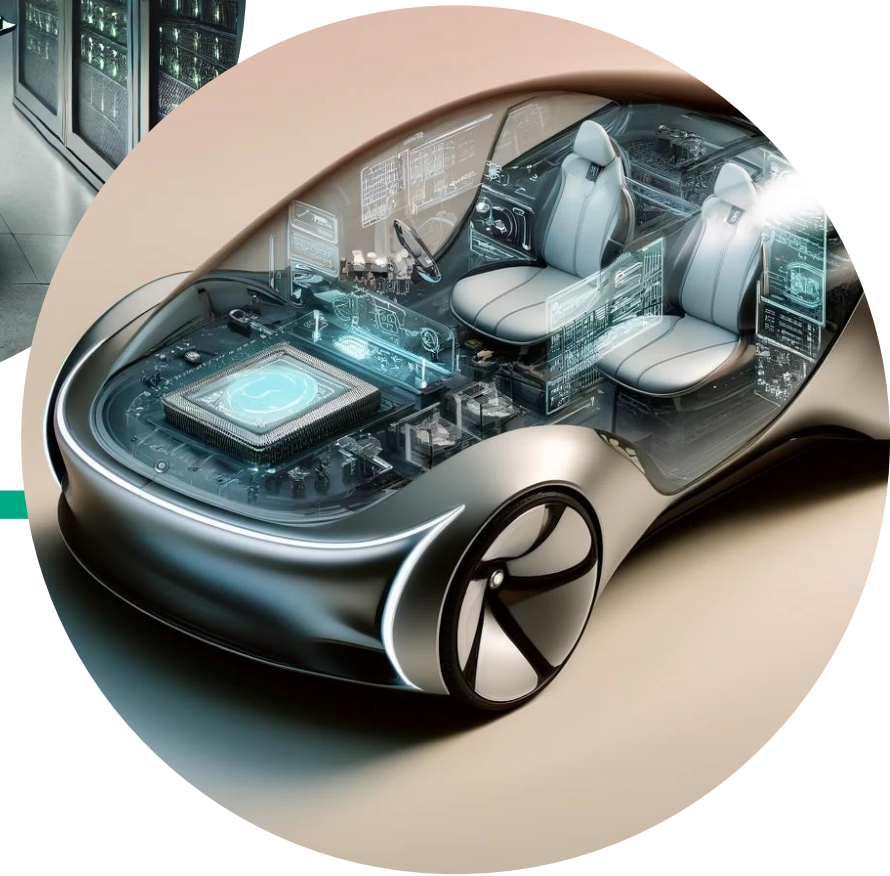
TTV = Package simplification, cost-efficient testing and increasing of testability



*TTC: Thermal Test Chip

Thermal Test Vehicle solutions at NANOTEST

From data centre to automotive



Development steps of Thermal Test Vehicles (TTV)

Design of customized TTV

We support our customers to verify their prospective package, TIMs and cooling solutions by offering TTV solutions

This includes:

- » Chip design and fabrication → Thermal test chips wafer
- » Chip configuration → Concept and feasibility
- » Design and manufacturing of substrate and ETB
- » Assembly and quality assessment
- » Measurement hardware
- » Measurement and control software
- » Calibration and qualification
- » Performance and reliability tests

All-in-one service:
From chip to TTV,
with full equipment
and testing support

Performance and reliability tests
Measurement Software
Measurement hardware



Thermal test chip wafer

Concept and feasibility

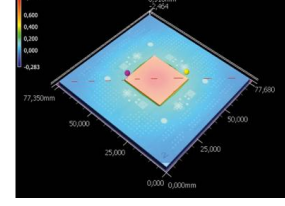
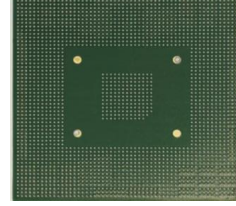
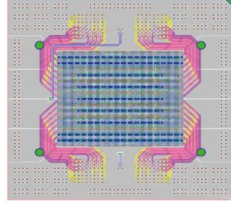
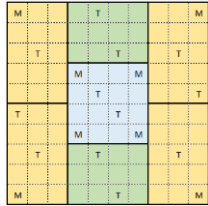
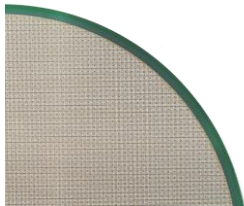
Substrate design

Substrate manufacturing

Chip and Board assembly

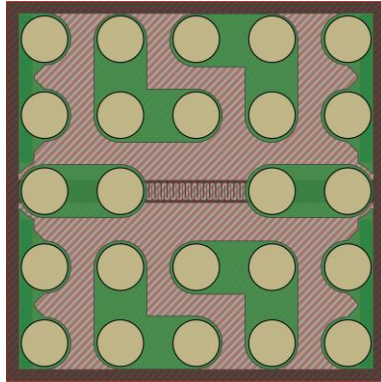
Quality control and test

Calibration



Off-the-shelf TTCs, TTVs and Control units

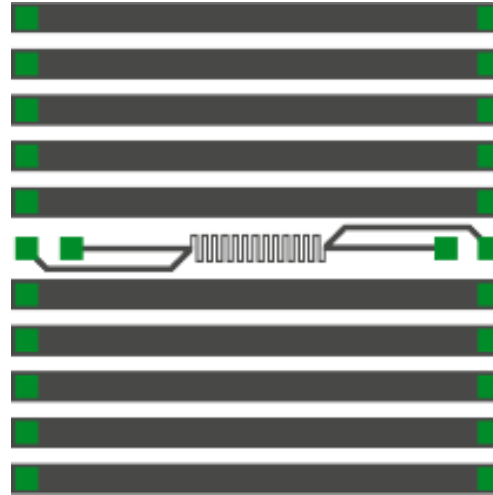
NT20-3k FC



Bumps

- » 2.4 x 2.4 mm² unit cells
- » 2 heaters, one RTD and 4 monitoring bumps
- » 8" wafer / > 4000 cells per wafer
- » Power Density: 10 W/mm²
- » Wafer thickness: 500 μm or 725 μm undoped silicon
- » Flip-chip assembly
- » 300 μm SAC bumps with 500 μm pitch
- » BSM
 - » Ti-NiV-Au (100nm-300nm-200nm)
 - » NiV-Pt-Au (300nm-100nm-200nm)
 - » Pure silicon

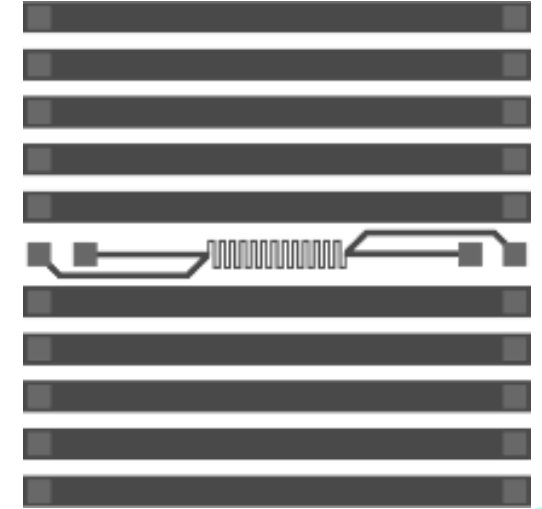
NT16-3k FC



Cu-pillar

- » 3.2 x 3.2 mm² unit cells
- » 10 heaters and one RTD
- » 8" wafer / > 2400 cells per wafer
- » Power Density: 10 W/mm²
- » Wafer thickness: 620 μm undoped silicon
- » Flip-chip assembly
- » 80 μm Cu-pillars with 300 μm pitch
- » without BSM

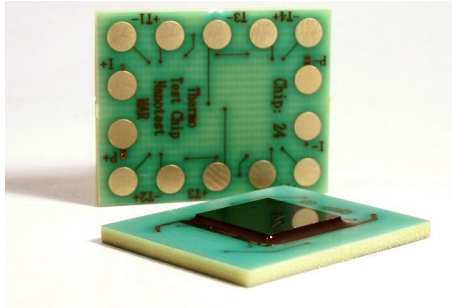
NT16-3k WB



Wire bond

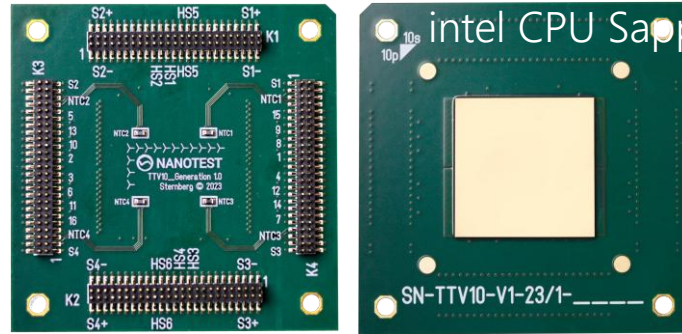
- » 3.2 x 3.2 mm² unit cells
- » 10 heaters and one RTD
- » 8" wafer / > 2400 cells per wafer
- » Power Density: 10 W/mm²
- » Wafer thickness: 400 μm undoped silicon
- » Wire-bond assembly
- » 150μm Aluminum pads
- » BSM: Ti-NiV-Au (100nm-300nm-200nm)

TTV5



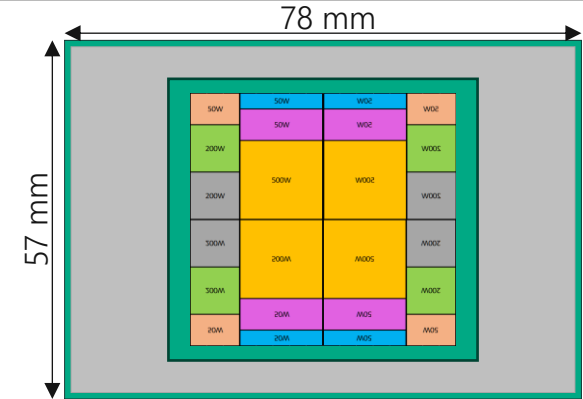
- » Based on the NT16-3k-FC
- » Chip size: 9.8 × 9.8 mm²
- » Substrate size: 25 × 20 mm²
- » Blank silicon surface
- » 5 temperature sensors (RTDs)
- » Uniform resistor heater
- » **Total power: 140W**

TTV10



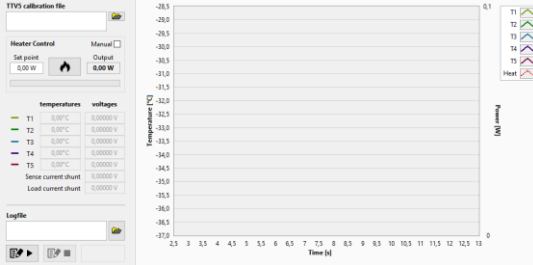
- » Based on the NT20-3k-FC
- » Chip size: 24.9 × 24.9 mm²
- » Substrate size: 60 × 60 mm²
- » Chip BSM: NiV-Pt-Au
- » 16 temperature sensors (RTDs)
- » 4 independent heater zones
- » **Total package power: 2000 W**

TTV16 (coming soon)*



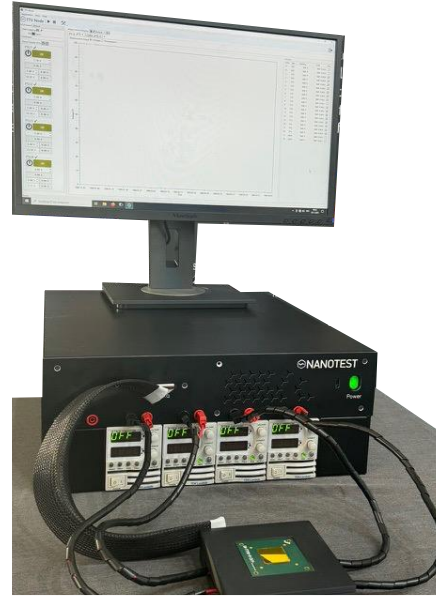
- » Based on the NT20-3k-FC
- » Chip size: 39.9 × 39.9 mm²
- » Available as single die or 4-dies chiplet
- » Substrate size: 78 × 57 mm²
- » Chip BSM: Ti-NiV-Au
- » 56 temperature sensors (RTDs)
- » 24 independent heater zones
- » **Total package power: 4000 W**

Control unit for TTV5



- » Hardware-software combination
- » Designed for NT16-TTV5
- » Features:
 - » Heater control (automatic / manual)
 - » Temperature monitoring
 - » Data logging

Control unit for TTV10



- » Controlling of power suppliers
- » Measurement and visualisation of RTDs
- » Scheduling for active power and temperature cycles
- » 19" case (stand-alone and integrable)
- » 4 programmable PSU
- » DAQ with 8 analog channels

Control unit for TTV16*

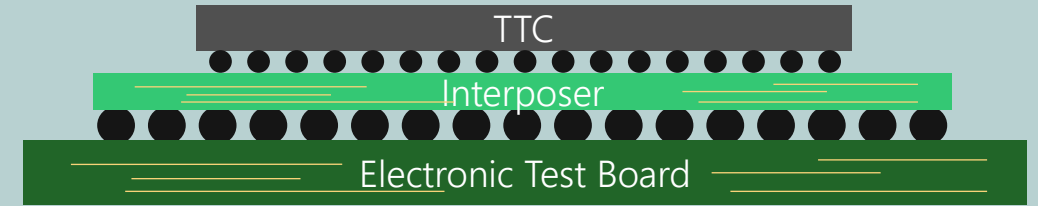
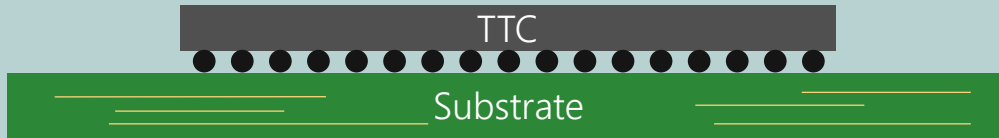


Customized TTV Design and Manufacturing

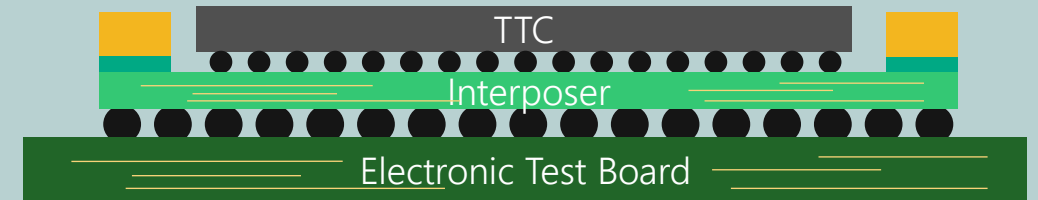
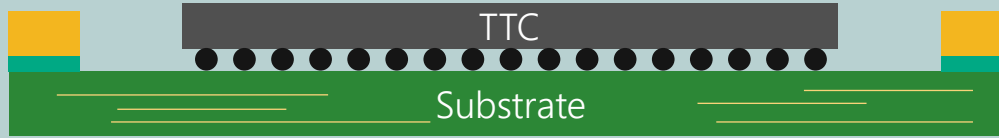
TTV without interposer

TTV with interposer

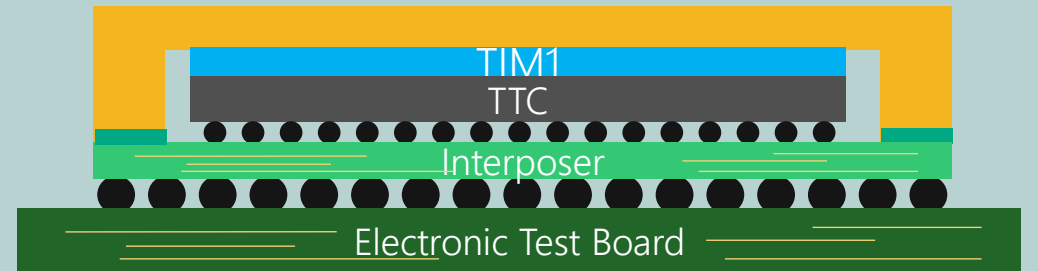
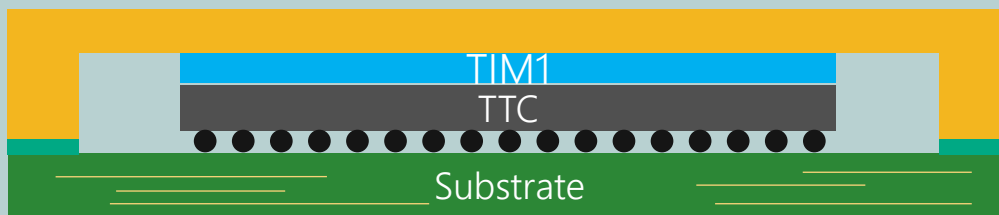
LID less TTV

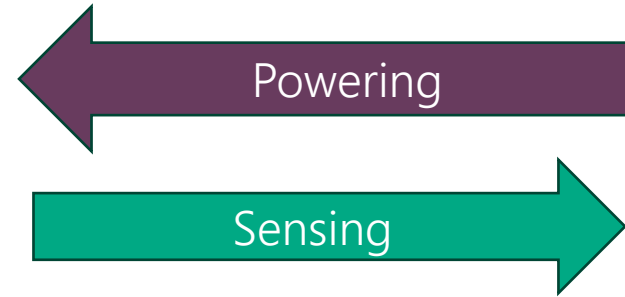
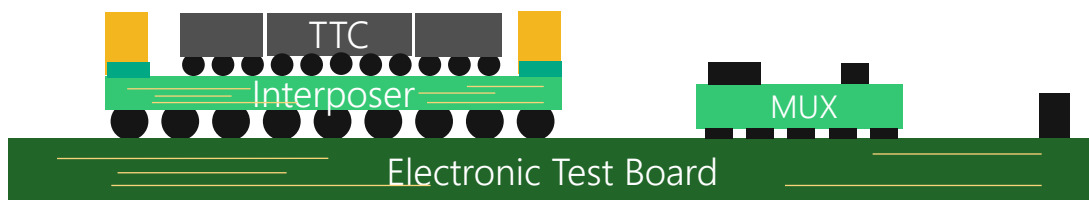
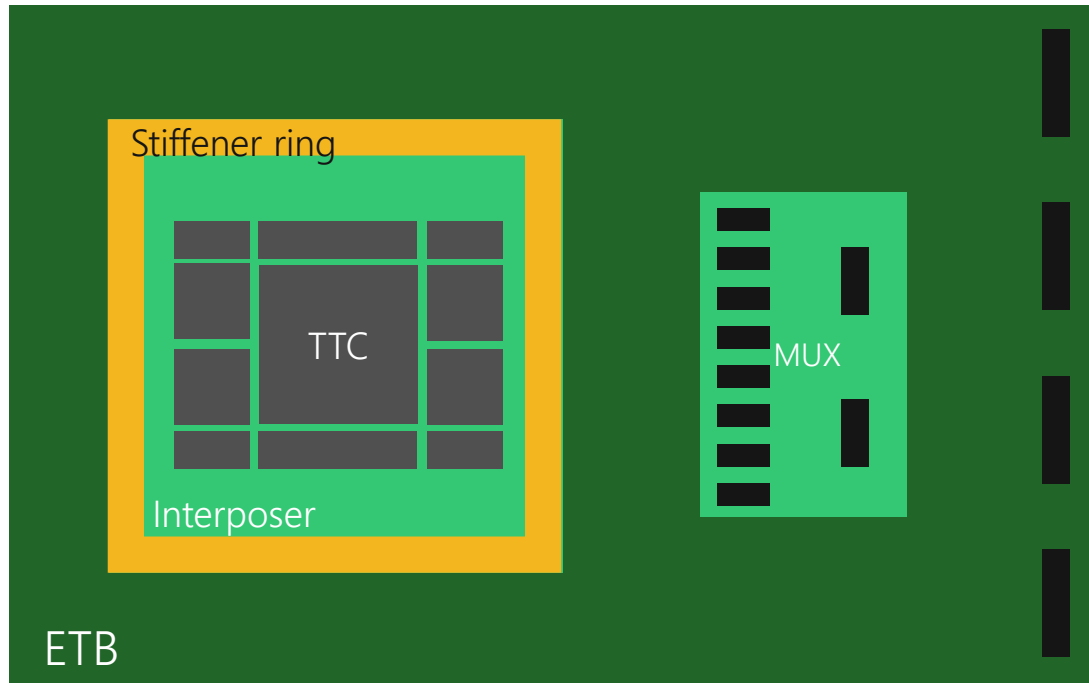


LID less TTV w/
stiffener ring



LIDDED TTV



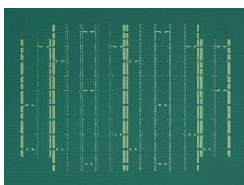


Control unit (PSUs, DAQ, PC)

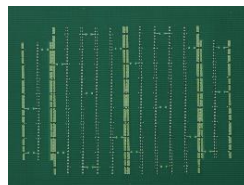




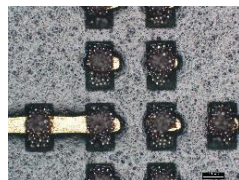
Incoming inspection



Solder application by stencil printing



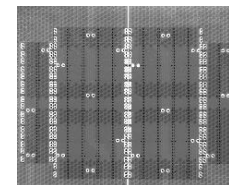
Optical inspection



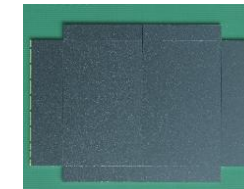
Chip assembling



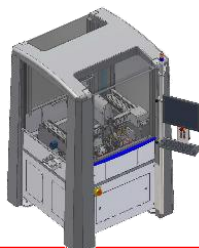
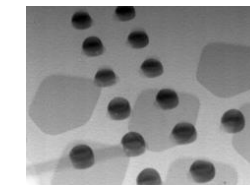
X-ray inspection



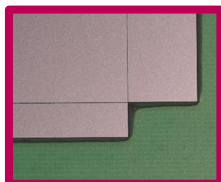
Reflow



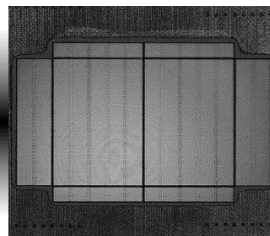
X-ray inspection



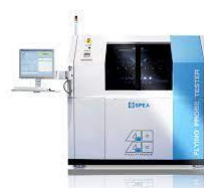
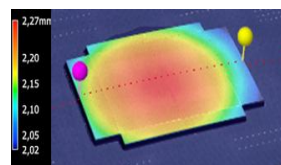
Underfill



CSAM inspection



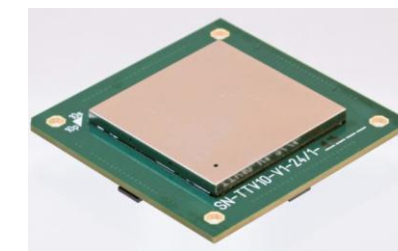
Optical inspection Warpage



Final electrical test



TTV

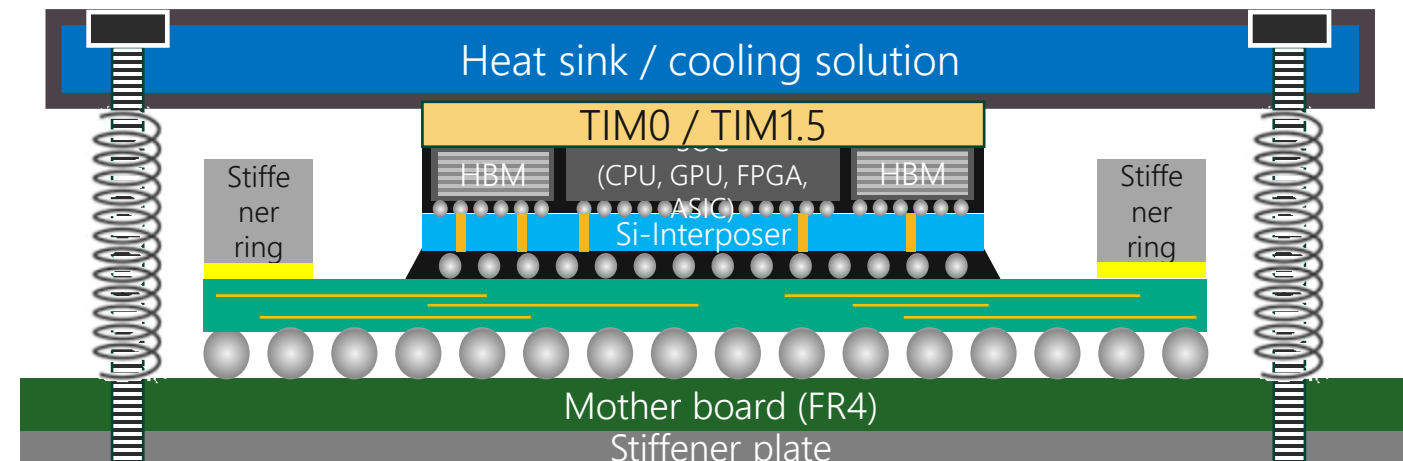
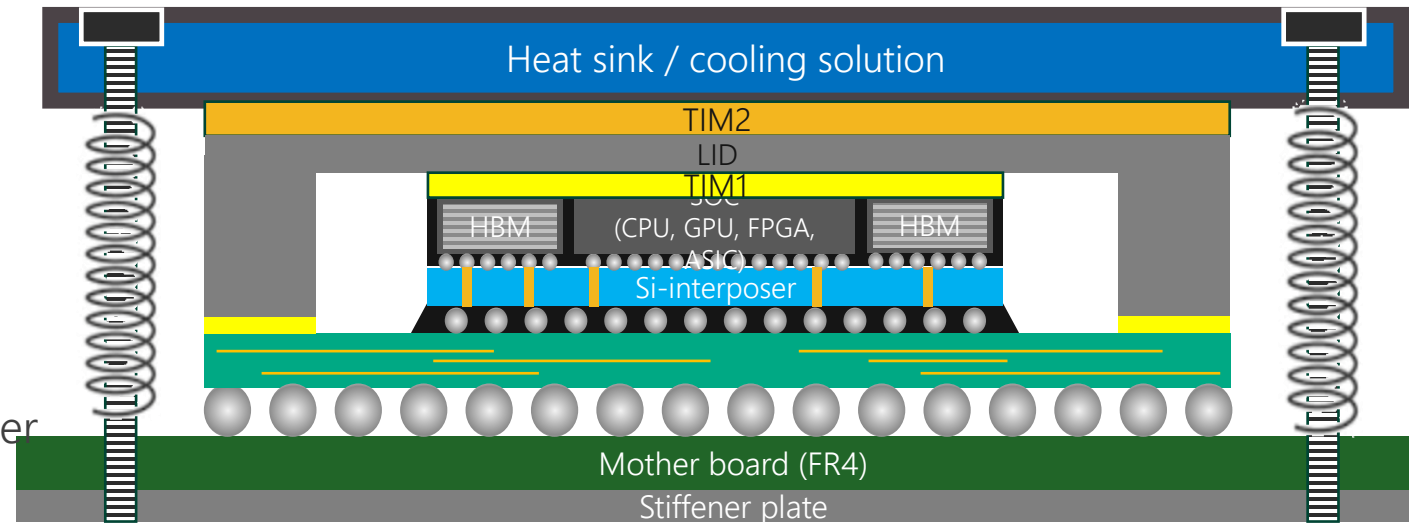


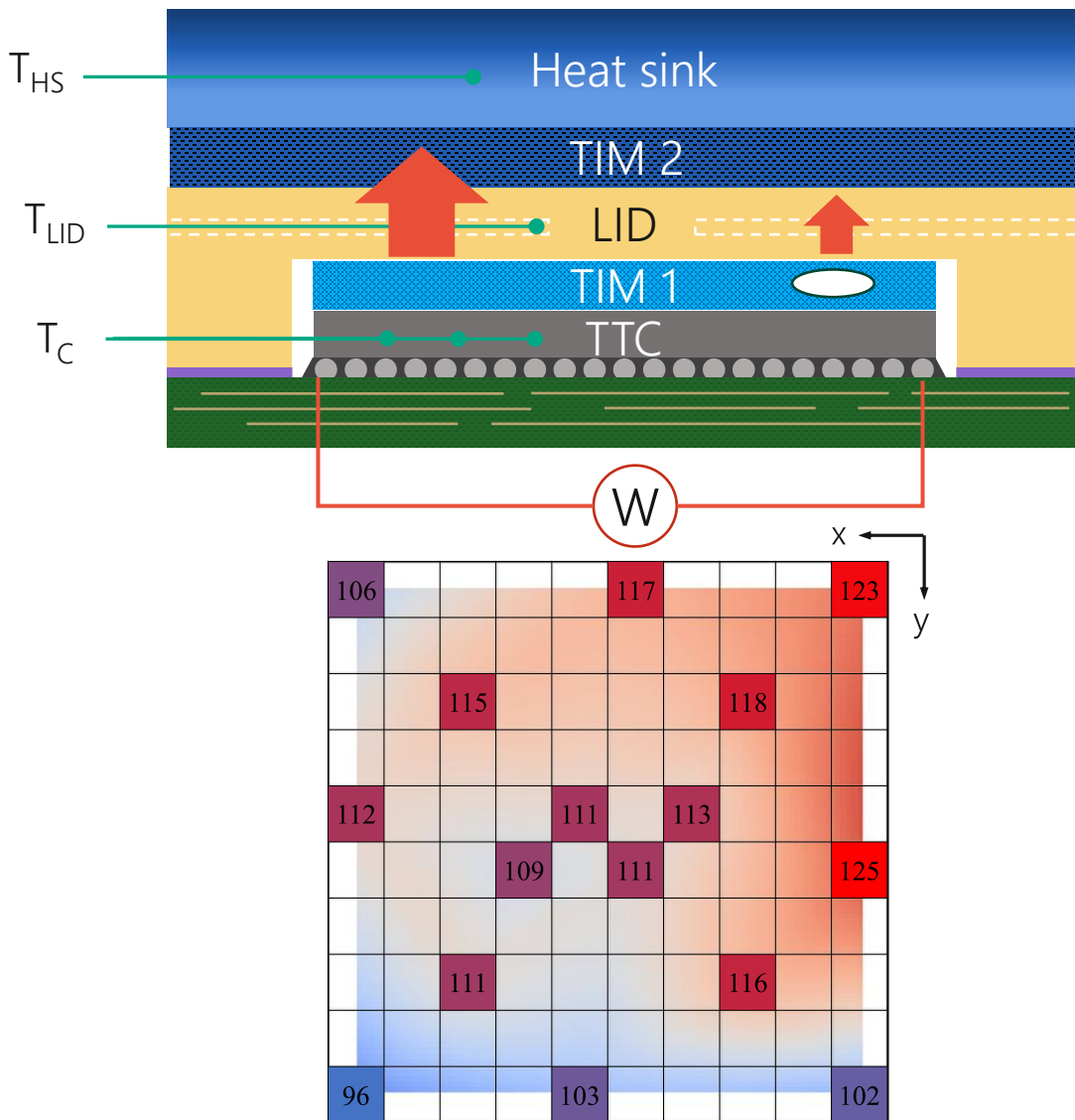
LID assembly

Characterization and test service

Package characterization, TIM characterization, power cycles, cooler performances

- » **TIM1** is applied between the silicon die and LID
- » Typical TIM1 are PCM, gel, grease or metallic TIM
- » Typical applications: Data centre, HPC.
- » Typical BLT: 20-50 μ m
- » **TIM2** is applied between LID and heat sink
- » Typical TIM2 are grease, pad, graphite sheet, gap filler
- » Typical applications: data centre, HPC.
- » Typical BLT: 100 - 300 μ m
- » **TIM1.5** (sometime called TIM0) are applied directly between the silicon die and the external heat sink in lid-less packages.
- » Typical TIM1.5 are PCM, grease or metallic TIM
- » Typical applications: smart phones laptops
- » Typical BLT: 50-100 μ m





$$R_{th,total} = \frac{T_C - T_{HS}}{P}$$

$$R_{th,TIM1} = \frac{T_C - T_{LID}}{P}$$

$$R_{th,TIM2} = \frac{T_{LID} - T_{HS}}{P}$$

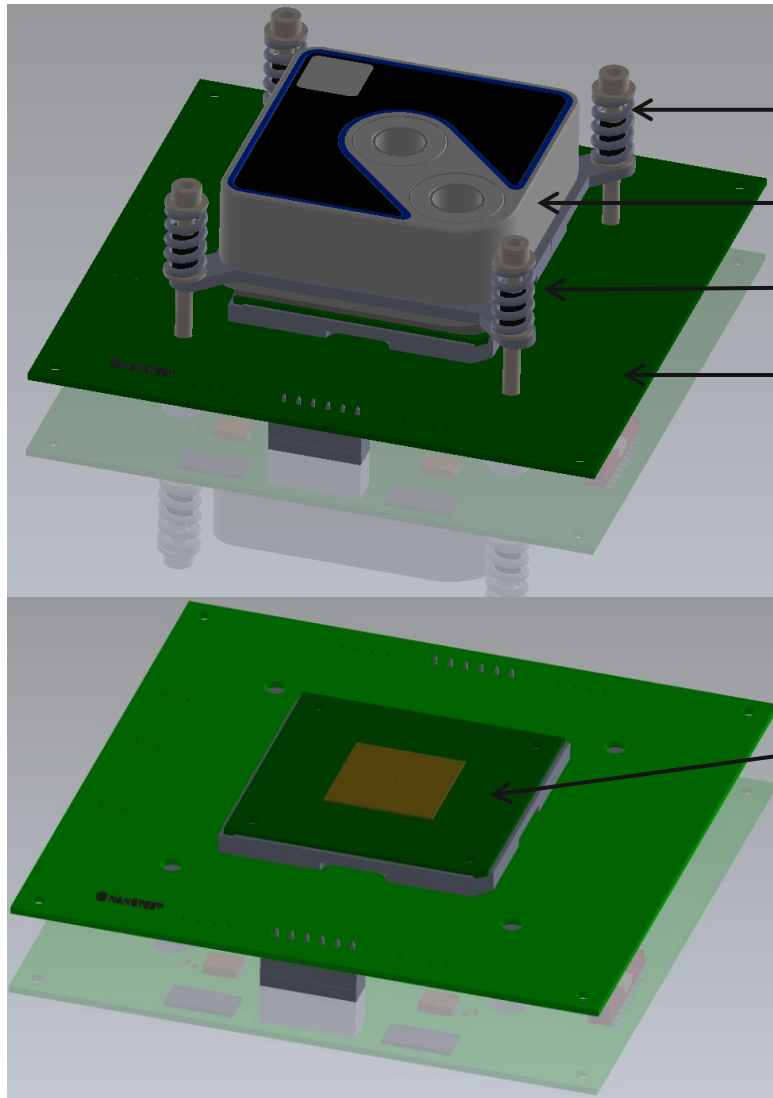
$$R_{th,die} = \frac{\Delta \bar{T}}{P} = 0.144 \frac{K}{W}$$

$$R_{th}(x, y) = \frac{\Delta T}{P_{cell}}$$

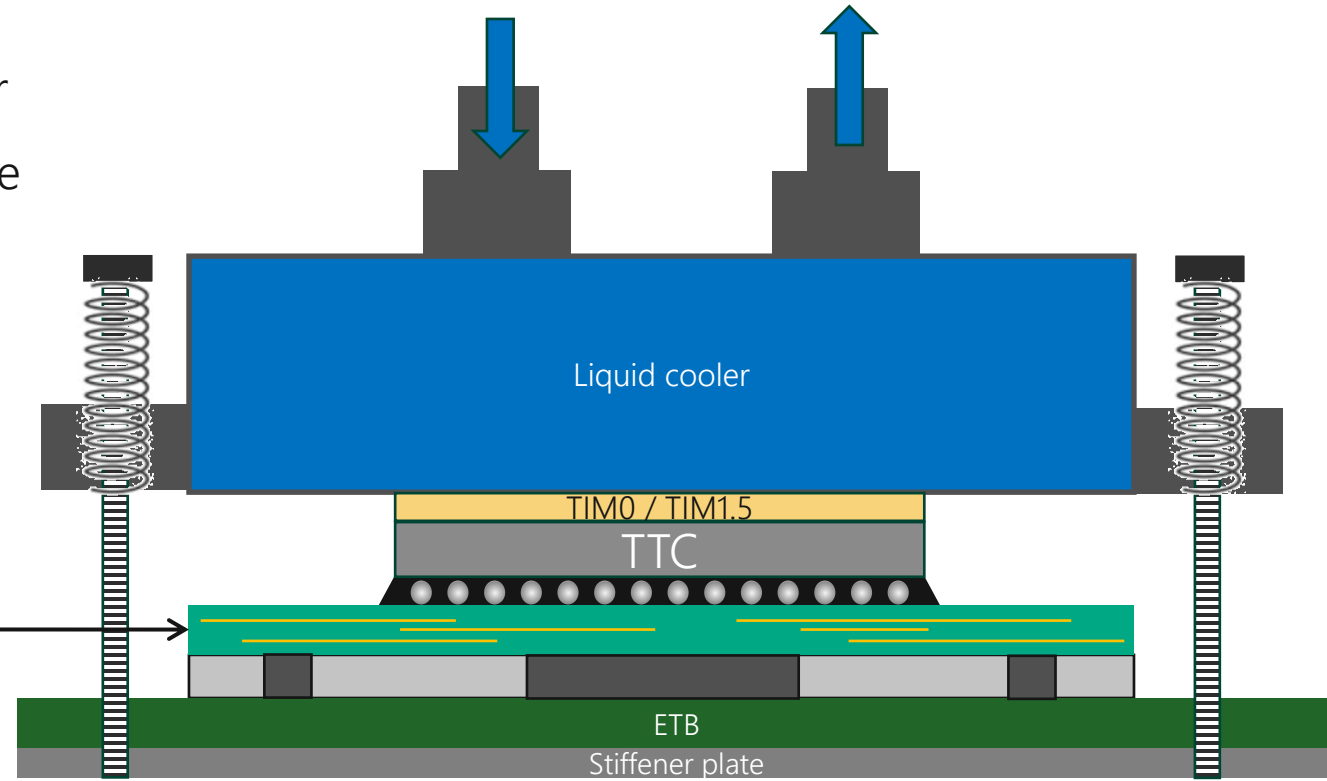
$$R_{th,min} = 12 \frac{K}{W}$$

$$R_{th,max} = 16.5 \frac{K}{W}$$

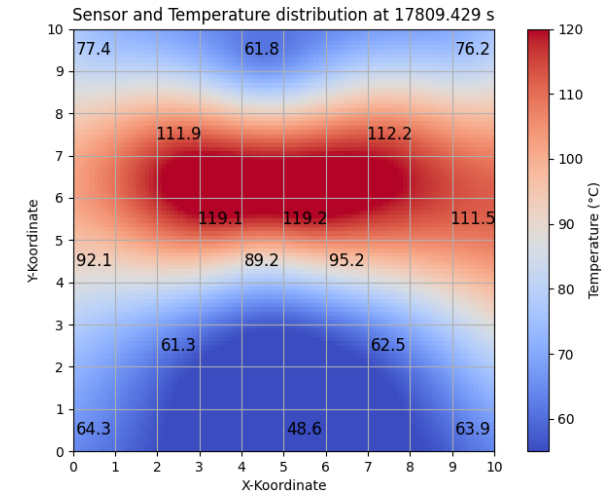
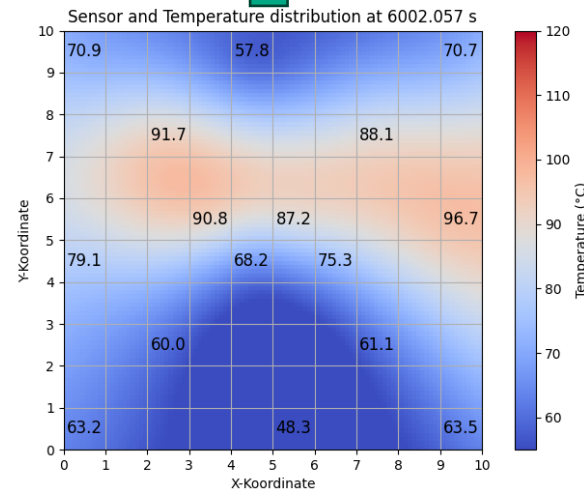
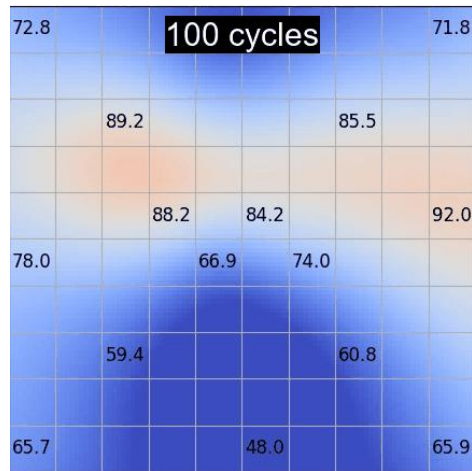
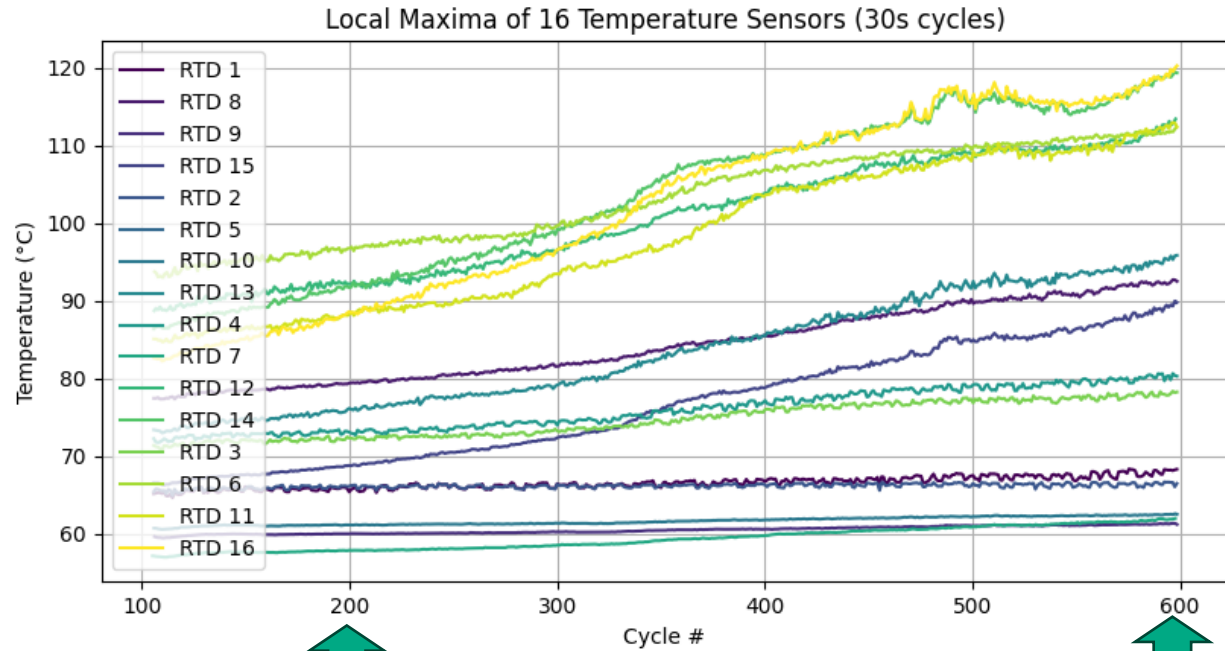
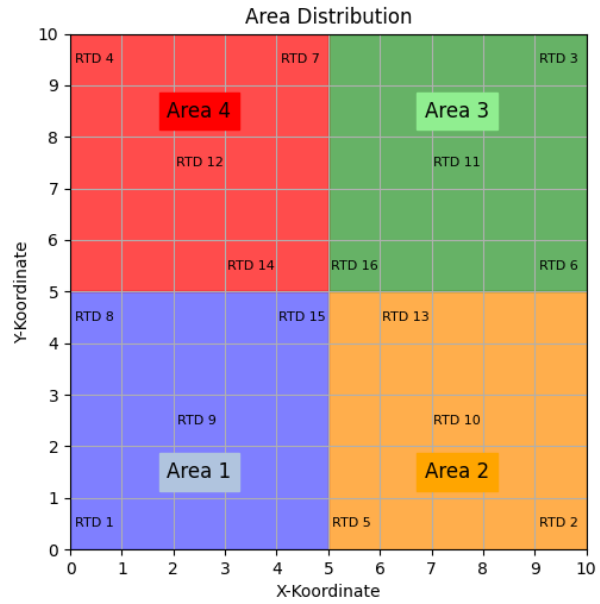
- » Steady state testing is a **simple way** for:
 - » Determination of maximum power $P=f(T)$
 - » Investigation of cooling performance
 - » Investigation of TIM performance
 - » Determination of thermal resistance



Spring
Liquid cooler
Stiffener plate
ETB



TTV10



- » We support our customers to verify their prospective package, TIMs and cooling solutions by offering TTV solutions
- » Three types of thermal test chips are available (bump, Cu-pillar and wire-bond)
- » Our comprehensive TTV solutions include everything from die and substrate design to assembly, quality assessment, measurement hardware and software, calibration, and testing.
- » We provide a range of TTV options readily available, including measurement equipment, ensuring a seamless verification process for our customers.



With more than a decade of hands-on experience, we've perfected the development, realization, and testing of thermal test vehicles.



nanotest.eu

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