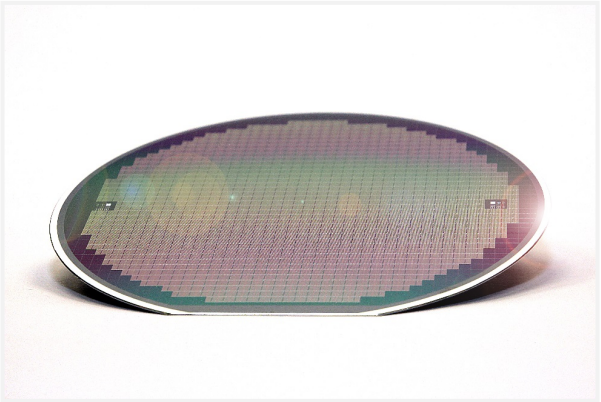
## Description

The NT16-3K Thermal Test Chip is designed as a modular system to provide the maximum of flexibility for thermal characterization and qualification of materials, packages and systems.

The smallest full functional chip cell of 3.2 mm x 3.2 mm consists of 10 heating resistors, which provide uniform heating and a resistor temperature sensor in the center. Heaters as well as temperature sensor are fabricated using only one Titanium layer as adhesion and barrier layer.

The chip can be used in any desired matrix, such as square or rectangular. All temperature sensors, whether in a single cell or arrayed cell configuration, can be individually addressed, allowing localized temperature measurements. The heating resistors on each chip cell can be powered individually in a serial or parallel configuration to achieve costumers and applications specific electrical resistance values and heat dissipations.



## Technical Specification

### Technology and Methodology

| | | |
|---|---|---|
| Fabrication technology | Thin Film | |
| Assembly technology | Wirebond technology | |
| Sensor | Resistance thermometer | |

### Wafer

| | | |
|---|---|---|
| Wafer material | Silicon with glass passivation | |
| Wafer size | 150 | mm |
| | 6 | inch |
| Wafer thickness | 400 | µm |
| Cell size | 3.2 x 3.2 | mm² |
| Scribe line between cells | 100 | µm |
| Matrix | up to 20 x 20 cells (66 x 66 mm²) | |
| Backside metallization | Ti/Pt/Au | |
| Backside metal thickness | 100/100/100 | nm |

### Heater

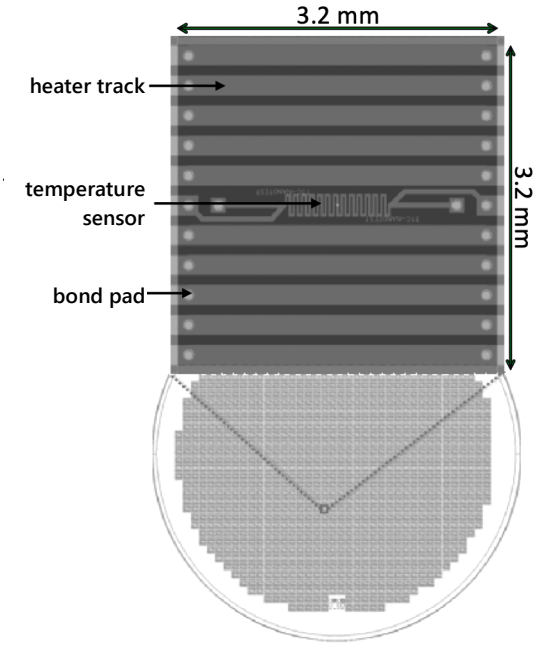
| | | |
|---|---|---|
| Heater type | resistor | |
| Resistors per chip | 10 | |
| Resistance per resistor | 160 | Ω |
| Max current per heater line | 400 | mA |
| Max power per cell | 250 * | W |
| Active heater area | > 62% of cell area | |
| Maximum temperature | 350 ** | °C |

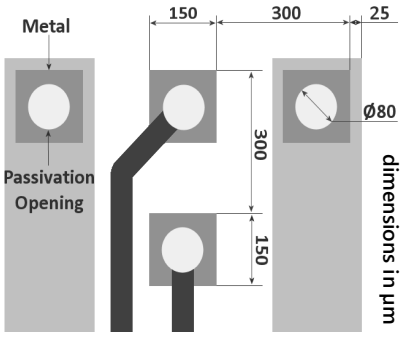
### Sensor

| | | |
|---|---|---|
| Sensor type | meander-structured resistor | |
| Sensor position | cell center | |
| Sensing method | four-terminal sensing | |
| Resistance value | 3 | kΩ |
| Sensitivity | 8 | Ω/K |
| | 8 mV/K @ 1mA | |
| Lateral size | 870 | µm |

### Assembly

| | | |
|---|---|---|
| Assembly technology | Wirebond technology | |
| Bond pad metallization | Al | |
| Pad size | 150 | µm |
| Pad raster | 300 | µm |




* high power dissipation is only possible to achieve with proper cooling

** 350°C operating temperature only applies to the chip itself. A much lower maximum operating temperature is likely due to other assembly components (i.e. PCB and solder) and has to be regarded.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## Chip selection guide

You can calculate the length of the chip edge depending on the number of cells per row / column using the following formula.

edge length = n x **cellLength** + (n-1) **scribeLineLength**
edge length = n x **3.2 mm** + (n-1) x **0.1 mm**

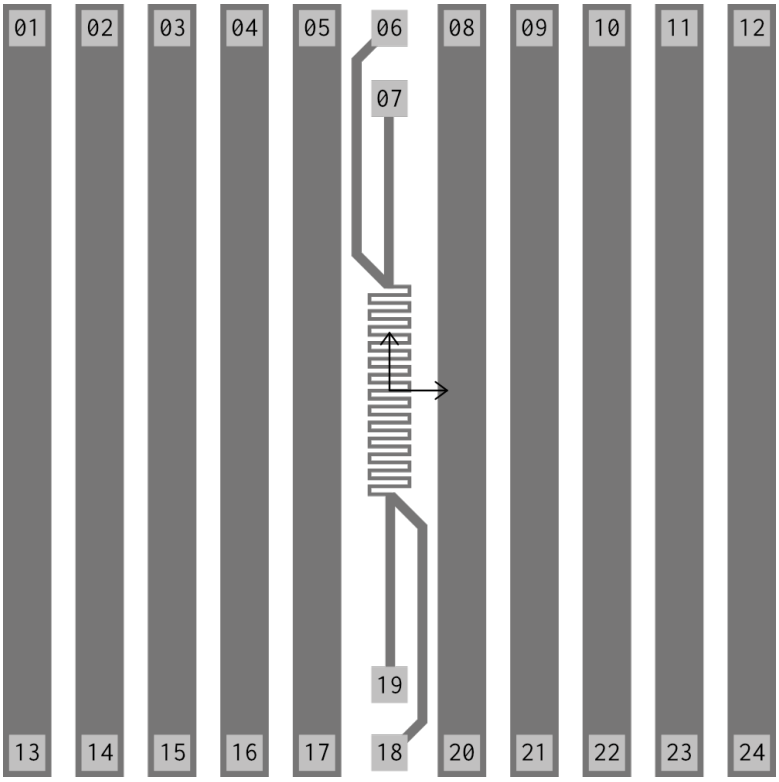
**Example: (3 x 3 matrix of cells)**

edge length = 3 x 3.2 mm + (n-1) 0.1 mm
chip size = 9.8 x 9.8 mm²

## Pin configuration

For absolute coordinates of each pin the point of origin (X=0, Y=0) is the cell center. Nomenclature of pins is involving a prefixed letter which indicates the purpose if the specific pin. Hx pins for connection to heating structures, pins SI for sensing current input and SV pins for voltage sensing.

| # | Name | X [µm] | Y [µm] |
|---|---|---|---|
| **01** | H1 | -1500 | 1500 |
| **02** | H2 | -1200 | 1500 |
| **03** | H3 | -900 | 1500 |
| **04** | H4 | -600 | 1500 |
| **05** | H5 | -300 | 1500 |
| **06** | SI | 0 | 1500 |
| **07** | SV | 0 | 1200 |
| **08** | H6 | 300 | 1500 |
| **09** | H7 | 600 | 1500 |
| **10** | H8 | 900 | 1500 |
| **11** | H9 | 1200 | 1500 |
| **12** | H10 | 1500 | 1500 |
| **13** | H1 | -1500 | -1500 |
| **14** | H2 | -1200 | -1500 |
| **15** | H3 | -900 | -1500 |
| **16** | H4 | -600 | -1500 |
| **17** | H5 | -300 | -1500 |
| **18** | SI | 0 | -1500 |
| **19** | SV | 0 | -1200 |
| **20** | H6 | 300 | -1500 |
| **21** | H7 | 600 | -1500 |
| **22** | H8 | 900 | -1500 |
| **23** | H9 | 1200 | -1500 |
| **24** | H10 | 1500 | -1500 |




## Application remarks

All offered dies are supposed to be used for characterization purposes. The application of the data from the test die to a functional system lies in the responsibility of the user. Nanotest makes no warranty, express or implied including the implied warranties of merchantability and fitness for a particular purpose, that the user's system designed using that data will perform as intended.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