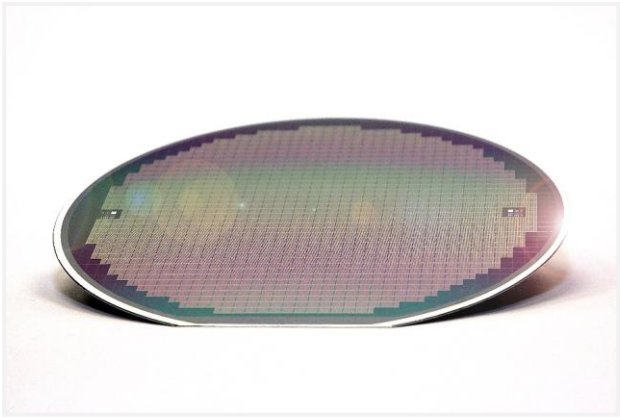
Description

The NT16-3K Thermal Test Chip is designed as a modular system to offer maximum flexibility for thermal characterization and qualification of materials, packages and systems.

The smallest fully functional chip cell of 3.2 mm x 3.2 mm consists of 10 uniform heating resistors and a thermistor in the center. Both the heating resistors as well as temperature sensor are fabricated in one layer.

The chip can be configured in any desired matrix. Each temperature sensor can be addressed individually, allowing localized temperature measurements. The heating resistors on each chip cell can be powered individually in a serial or parallel configuration to achieve costumer and application specific electrical resistance values and heat dissipation.



Technical Specification

Technology and Methodology

Fabrication technology	Thin film	
Assembly technology	Flip chip	
Sensor	Resistance thermometer	

Wafer

Wafer material	Silicon, undoped	
Wafer size	200	mm
	8	inch
Wafer thickness	620	µm
Cell size	3.2 x 3.2	mm^2
Scribe line between cells	100	µm
Topside passivation	7 µm Pi (polymer passivation)	
Backside metallization	Option A	Ti-NiV-Au (100nm-300nm-200nm)
	Option B	Non
Unit cell count	2400	

Heater

Heater type	Resistor	
Resistors per chip	10	
Resistance per resistor	160 ± 10	Ω
Max current per heater	0.25	A
Max power per cell	100	W
Max power density	10	W/mm^2
Active heater area	62% of cell area	

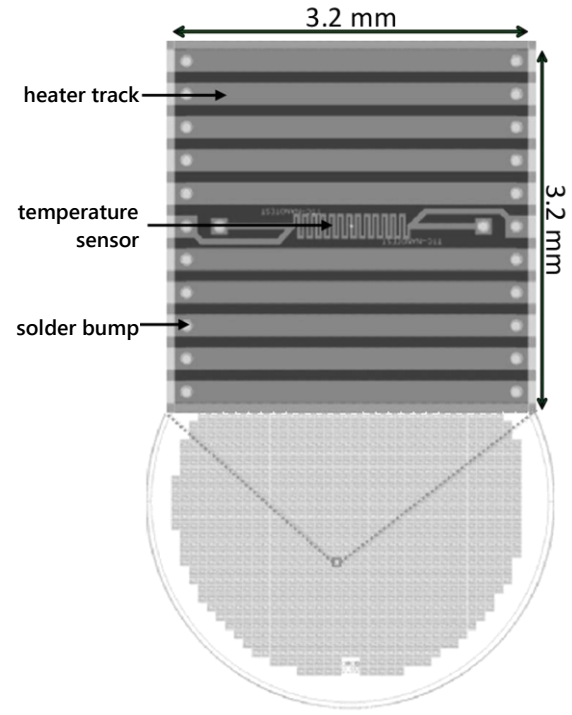
Sensor

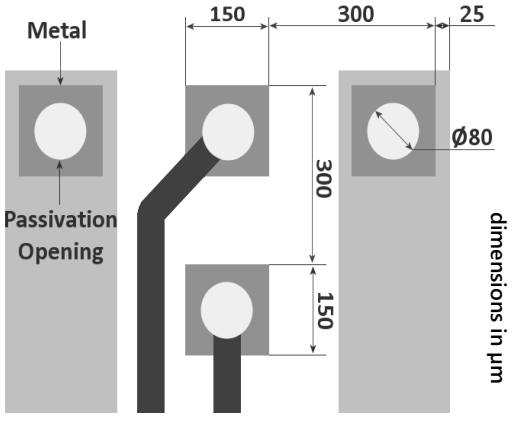
Sensor type	meander-structured resistor	
Sensor position	cell center	
Sensing method	four-terminal sensing	
Resistance value	3.0 ± 0.2	kΩ
Sensitivity	10.0 *	Ω/K
Lateral size	870 x 200	µm

Assembly

Assembly technology	Flip chip	
Interconnect type	Cu-Pillar (40 µm) with SnAg (30 µm)	
Interconnect diameter	80	µm
Pad pitch	300	µm

* theoretical value based on the Ti temperature coefficient.





Chip selection guide

The length of the chip edge as a function of the number of cells per row / column can be calculated using the following formula.

edge length = n x cellLength + (n-1) scribeLineLength
edge length = n x 3.2 mm + (n-1) x 0.1 mm

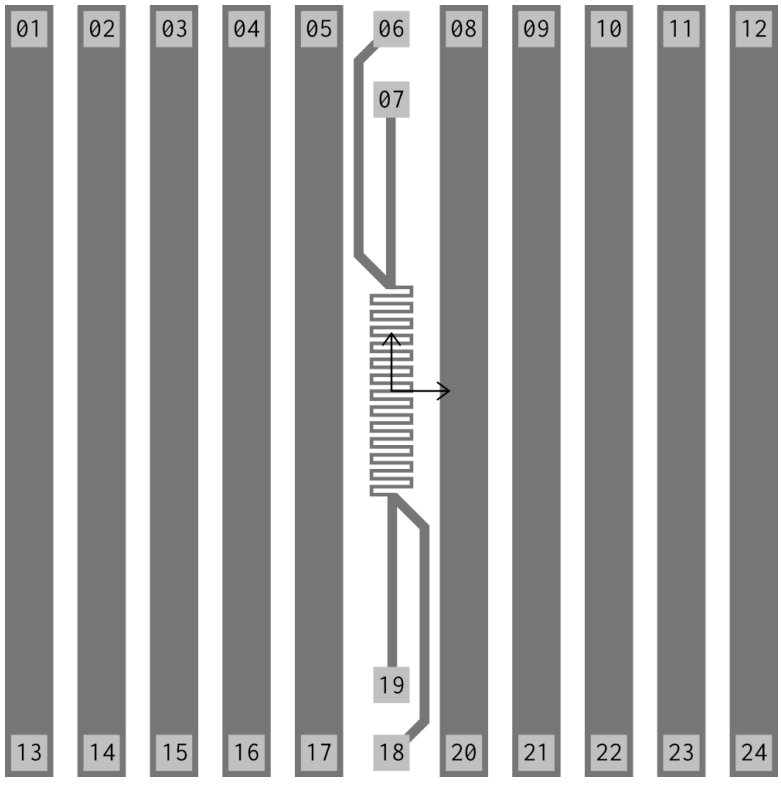
Example: (3 x 3 matrix of cells)

edge length = 3 x 3.2 mm + (3-1) x 0.1 mm
chip size = 9.8 x 9.8 mm²

Pin configuration

For absolute coordinates of each pin the point of origin (X=0, Y=0) is the cell center. Nomenclature of pins is involving a prefixed letter which indicates the purpose if the specific pin. Hx pins for connection to heating structures, pins SI for sensing current input and SV pins for voltage sensing.

#	Name	X [µm]	Y [µm]
01	H1	-1500	1500
02	H2	-1200	1500
03	H3	-900	1500
04	H4	-600	1500
05	H5	-300	1500
06	S1	0	1500
07	S1	0	1200
08	H6	300	1500
09	H7	600	1500
10	H8	900	1500
11	H9	1200	1500
12	H10	1500	1500
13	H1	-1500	-1500
14	H2	-1200	-1500
15	H3	-900	-1500
16	H4	-600	-1500
17	H5	-300	-1500
18	S2	0	-1500
19	S2	0	-1200
20	H6	300	-1500
21	H7	600	-1500
22	H8	900	-1500
23	H9	1200	-1500
24	H10	1500	-1500



Handling and storage

It is recommended to handle the wafers only with suitable tools and only with gloves. The solderability of the contacts strongly depends on the storage conditions. To prevent oxidation/corrosion of the contacts and moisture-induced defects to the polymer passivation during processing, the wafer should be stored at room temperature in a dry and low-oxygen atmosphere. The use of a nitrogen storage cabinet is recommended.

Application remarks

All offered dies are supposed to be used for characterization purposes. The application of the data from the test die to a functional system lies in the responsibility of the user. Nanotest makes no warranty, express or implied including the implied warranties of merchantability and fitness for a particular purpose, that the user's system designed using that data will perform as intended.